Abstract
The most recent version (C2M™) of Silicon Carbide (SiC) devices is used in a Zero Voltage Switching (ZVS) converter application. A 1200V, 160mohm SiC MOSFET from Cree Inc. is used to design a high-frequency ZVS LLC resonant full-bridge (FB) DC/DC converter. With the outstanding advantages of SiC MOSFET, which has lower junction capacitance and low-on-state resistor compared to a silicon (Si) device, the resonant converter can achieve a high-frequency and high-efficiency, thus increasing the power density with fewer components and reducing total cost. An 8kW prototype is developed to demonstrate how the SiC MOSFET can help achieve the highest performance for a soft-switching DC/DC converter with the maximum efficiency measured at 98.3 percent. These types of converters can be commonly used in three-phase industrial power supply applications. These include telecom or server power converters, high-voltage DC (HVDC) systems, inductive heatings or electric vehicle (EV) chargers.

Introduction: Conventional High-Power Isolated DC/DC converter
Currently, in three-phase, medium-to-high-power industrial electronics applications, such as telecom AC/DC power, HVDC system, EV charger etc., there are mainly two silicon-based soft-switching topologies used for isolated DC to DC stages after the three-phase PFC, which has high-DC output voltage ranged from 600 Vdc to 800 Vdc.

Figure 1: Three-level (TL) DC/DC converter with 600V Silicon MOSFET
The first topology is the three-level (TL) DC/DC converter as shown in Figure 1. This TL technique has been applied to DC/DC converters since 1992 [1] to reduce the voltage stress of the switches. The key benefit of a TL DC/DC converter is the fact that it can use low-voltage stress devices with two series-connected, like a 600V MOSFET, to switch high-DC link input voltage. The TL DC/DC converter uses phase-shift control or resonant control to achieve soft-switching. However, this TL technique has some limitations. Firstly, it needs complicated control and driver for at least eight switches used. Secondly, two switches connected in series are used to replace a single switch, which results in high-conduction losses. Thirdly, the clamping diodes and voltage sources are introduced to maintain an equal voltage stress distribution among these two series switches to account for the presence of intrinsic differences among devices. The clamping voltage source is equal to the voltage stress magnitude of the basic converter, which is half of the original voltage stress applied on the switches. Lastly, with two series-connected devices, the dead-time between high-side and low-side should be large enough to account for the parametric variations in devices, such as rise time, fall time and turn-on/turn-off delay time. This limits the switching frequency at or below 200 kHz.

The second common Si-based topology is an interleaved two-Level DC/DC converter (or input-series-output-parallel connected DC/DC Converter) as shown in figure two. The input voltage after PFC has a neutral point to derive input DC link voltage with positive (+400Vdc) and negative (-400VDC). Two separated two-level full-bridge DC/DC converters with interleaved switching are implemented to convert high-input voltage to output. Because of low-DC input voltage of 400V, low-stress voltage devices, such as 600V Si MOSFET, can be used. But, similar to the three-level DC/DC converter, the interleaved two-level converter has a complicated control and driver implementation. Moreover, with two H-bridge converters in series on the primary side, the balance between positive voltage and negative voltage is a challenge, and a special control approach should be applied to balance primary voltage and current between these two H-bridge converters, otherwise, it leads to over-stress on one of the bridge converters. A work-around to solve this issue has been developed, but it adds cost and complicates the circuit design [2].

In summary, the disadvantages of these topologies are:

- Complex Control and Driver
- Difficult to Balance between Primary Voltage and Negative Voltage
- More Devices
- Lower Reliability

![Interleaved Two-Level H-bridge DC/DC converter with 600V Silicon MOS](image)

*Figure 2: Interleaved Two-Level H-bridge DC/DC converter with 600V Silicon MOS*
High-Frequency Full Bridge ZVS LLC Resonant Converter with 1200V SiC MOSFET

In this paper, a C2M™ 1200V 160mohm SiC MOSFET from Cree Inc. is used to design a high-frequency two-level full bridge (or H-bridge) ZVS LLC resonant converter as shown in figure three. With the high-blocking voltage, fast switching and low-loss characteristics of SiC devices, it can simplify the topology to a one H-bridge converter for a high-input voltage isolated DC/DC converter design.

![Circuit Diagram]

Figure 2: Proposed Two-Level H-Bridge LLC ZVS DC/DC Converter with 1200V SiC MOS

<table>
<thead>
<tr>
<th>Item</th>
<th>SiC MOSFET C2M0160120D</th>
<th>Si MOSFET SPW47N60CFD</th>
<th>Si MOSFET IPW65R110CFD</th>
</tr>
</thead>
<tbody>
<tr>
<td>Breakdown Voltage @Tjmax</td>
<td>1200V</td>
<td>650V</td>
<td>650V</td>
</tr>
<tr>
<td>Rdson @Tc=110°C</td>
<td>0.22Ω</td>
<td>0.14Ω</td>
<td>0.19Ω</td>
</tr>
<tr>
<td>Ciss @f=1MHz VDS=100V</td>
<td>527pF</td>
<td>7700pF</td>
<td>3240pF</td>
</tr>
<tr>
<td>Coss @f=1MHz VDS=100V</td>
<td>100pF</td>
<td>300pF</td>
<td>160pF</td>
</tr>
<tr>
<td>Crss @f=1MHz VDS=100V</td>
<td>5pF</td>
<td>10pF</td>
<td>8pF</td>
</tr>
<tr>
<td>Td(on)V Turn on delay time</td>
<td>7ns (VDD=800V)</td>
<td>30ns (VDD=400V)</td>
<td>16ns (VDD=400V)</td>
</tr>
<tr>
<td>Td(off)V Turn off delay time</td>
<td>13ns (VDD=800V)</td>
<td>100ns (VDD=400V)</td>
<td>68ns (VDD=400V)</td>
</tr>
<tr>
<td>Qg, typ</td>
<td>32.6nC</td>
<td>248nC</td>
<td>118nC</td>
</tr>
<tr>
<td>Body diode recovery time trr</td>
<td>35ns</td>
<td>210ns</td>
<td>150ns</td>
</tr>
<tr>
<td>Body diode charge Qrr</td>
<td>0.120uC</td>
<td>2uC</td>
<td>0.8uC</td>
</tr>
</tbody>
</table>

Table 1: MOSFET parameters’ comparison with TO-247 package

Table one compares MOSFET parameters with a TO-247 package. This package includes a 1200V 160mOhm SiC MOSFET and a high-performance Si 650V MOSFET. The cost-effective 1200V 160mohm SiC MOSFET on-state resistor (Rdson) at 110degC is larger than Si 650V MOS for Si-based topologies. There are two MOSFETs conducting current for each on-state compared to simple a two-level full-bridge topology using SiC. The SiC MOSFET can still have low-total Rdson and low-conduction losses compared to Si-based topologies. More importantly, 1200V SiC MOSFET brings the
following superior benefits on this soft-switching H-bridge topology.

Benefits:

- Low-parasitic capacitance Ciss, Coss and Crss allow devices fast switching to reduce turn-off switching losses; Therefore it has better switching performance and is more suited to use in very high-switching frequency converters.

- Low-body diode trr and Qrr reduce diode switching losses and electrical noise due to short reverse recovery time.

- Short-turn-on and turn-off delay time reduces dead time; small dead time induces low-device conduction loss and low-winding loss, thus improve efficiency.

- Low-Qg allows lower gate drive losses when switching frequency is high.

Because of low-parasitic capacitance of SiC MOSFET, the commutation dead time can be set low to allow less magnetizing energy to achieve ZVS condition. This often causes smaller resonant tank circuits with small magnetizing inductance Lm to discharge the parasitic capacitance of SiC MOSFET. The resonant frequency can be increased with SiC MOSFET even more than twice that of conventional Si-based topology. The below curve calculates the DC gain difference with different resonant tank when resonant frequency increases from fr=130 kHz to fr=260 kHz. The total resonant tank values are changed from Lm=150mH, Lr=35uH and Cr=40nF to Lm=100uH, Lr=15uH and Cr=25nF. With smaller resonant tank, the passive components' size and cost can be dramatically reduced.

![Figure 4: DC gain curves (left: Si MOSFET at fr=130 kHz; right: SiC MOSFET at fr=260 kHz)](image)

**Design Consideration of 8kW Full Bridge ZVS LLC Resonant Converter with 1200V SiC MOSFET**

A SiC-based 8kW two-level full bridge ZVS LLC resonant converter is developed to compare with conventional Si-based topologies.

<table>
<thead>
<tr>
<th>Items</th>
<th>Two-Level FB with SiC MOSFET at 260 kHz</th>
<th>Three-Level FB with Si MOSFET at 130 kHz</th>
<th>Interleaved Two-Level FB with Si MOSFET at 130 kHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>MOSFETs</td>
<td>8 pieces</td>
<td>16 pieces</td>
<td>16 pieces</td>
</tr>
<tr>
<td>2M01960120D</td>
<td>C2M01960120D</td>
<td>SPW47N800CDF</td>
<td>SPW47N800CDF</td>
</tr>
<tr>
<td>Magnetic transformer Lm</td>
<td>1 piece PQ2550</td>
<td>2 pieces PQ5050</td>
<td>2 pieces PQ5050</td>
</tr>
<tr>
<td>Resonant Inductor Lr</td>
<td>1 piece PQ3535</td>
<td>2 pieces PQ3535</td>
<td>2 pieces PQ3535</td>
</tr>
<tr>
<td>Resonant Capacitor Cr</td>
<td>25nF</td>
<td>35nF</td>
<td>35nF</td>
</tr>
<tr>
<td>MOS driver IC</td>
<td>4 pieces</td>
<td>8 pieces</td>
<td>8 pieces</td>
</tr>
<tr>
<td>MOS drive transformer</td>
<td>2 pieces</td>
<td>4 pieces</td>
<td>4 pieces</td>
</tr>
<tr>
<td>Clamping diodes</td>
<td>None</td>
<td>4 pieces</td>
<td>None</td>
</tr>
<tr>
<td>Balance circuitry</td>
<td>None</td>
<td>None</td>
<td>Yes</td>
</tr>
</tbody>
</table>

**Table 2: Key component comparisons with SiC MOSFET and Si MOSFET solutions.**
Component comparison between Si and SiC solutions

Table two compares the key component differences between Si and SiC topologies. With SiC MOSFET and high-resonant frequency at 260 kHz, the resonant tank is small with a lower components count. Also, the drive solution is simple compared to Si low-frequency solution at 130 kHz. This brings a lower system cost when using 1200V SiC MOSFET with high-resonant frequency.

Modes of Operation
Since the resonant LLC tank network gain is frequency modulated, the converter can operate in three conditions depending on input voltage and load current conditions.

Condition One
At resonant frequency operation with fs=fr, each half-cycle contains a complete power delivery operation, where the resonant half-cycle is completed during the switching half-cycle. By the end of the switching half-cycle, the resonant inductor current ILr equals to the magnetizing current ILM and rectifier current reaches zero. The resonant tank has unity gain and the best optimized operation and efficiency, therefore, the transformer turns ratio is designed such that the converter operates at this nominal input and output voltage. For this 8kW design, we are setting the nominal input voltage at 700Vdc with 270Vdc output voltage.

Condition Two
Above resonant frequency operation with fs>fr, each half-cycle contains a partial power delivery operation, similar to the resonant frequency operation, differing in that the resonant half-cycle is not completed and interrupted by the start of the other half of switching cycle, hence primary side MOSFETs have increased turn-off losses and secondary rectifier diodes have hard commutation. The converter operates in this mode at higher input voltage, where a step down gain or buck operation mode is required. For this 8kW design, it occurs above 700Vdc to 750Vdc input.

Condition Three
Below resonant frequency operation with fs<fr, each half-cycle contains a power delivery operation, at the time when resonant half-cycle is completed and resonant inductor current ILr reaches the magnetizing current, the freewheeling operation starts and carries on to the end of the switching half-cycle, hence primary sides have increased conduction losses due to the commutation circulating energy and diodes on the secondary side have ZCS operation. The converter operates in this mode at lower input voltage where step up gain or boost operation is required. At this 8kW design, it occurs below 700Vdc to 650Vdc input. In this condition, there is an additional mode when resonant current ILr drops equal to magnetizing current ILM to circulate on the primary side. It has some circulating conduction loss, but condition one and condition two do not have this mode. Figure five gives the timing and full cycle operation modes of this SiC MOSFET at condition three. For condition one and condition two, it is almost the same but no circulating mode between t2 to t3 and t5 to t6. Here, Lm represents equivalent magnetizing inductance of transformer T1.

Below, the positive half-cycle operation modes are explained from t0 to t3 and the negative half-cycle t3 to t6 works in a symmetrical manner to the positive half-cycle:

- During t0 to t1 period, assuming Q2/Q3 turn off at t0, the primary current is in reverse, before Q1/Q4 turn on for a short dead time, the current is conducting through the body diodes of Q1/Q4. The magnitude of the resonant inductor current ILr is greater than the magnetizing current ILM. As such, the top coil of the transformer T1 provides the output current to the load through the diode DR1. Body diodes are conducted before Q1/Q4 turned on, and Q1/Q4 can achieve turn-on ZVS condition. The current flows in reverse through SiC MOSFET Q1/Q4 when it is turned on, is referred to as third quadrant operation. Because of low-parasitic capacitance, the SiC MOSFET solution allows a short dead time with less circulating current on the primary to improve efficiency.

- During t1 to t2 period, at time t1, the resonant inductor current ILr goes to zero and allow the primary current IP to reverse direction. As such, the primary current flows in a forward (or normal direction) through the channels of the transistors Q1/Q4. The magnitude of the resonant inductor current ILr keeps greater than the magnetizing current ILM. As such, the top coil of the transformer T1 provides the output current to the load through the diode DR1.

- During t2 to t3 period, resonant current ILr drops to equal the magnetizing current ILM, and both DR1 and DR2 are blocked. The Lr and Lm join to resonate together with capacitance Cr to discharge C2/C3 and charge C1/C4 for the upcoming negative half-cycle, and then it moves to the next symmetrical negative half-cycle from t3 to t6.
Figure 5: Timing and full cycle operation modes of this SiC MOSFET ZVS converter
A SiC MOS-based prototype of an 8kW ZVS LLC resonant full-bridge converter is developed. Input voltage is from 650Vdc to 750Vdc, output voltage is 270Vdc with 30A output current. Targeted efficiency is above 98 percent with resonant frequency at 260 kHz. The size of the prototype board as shown in the below figure is 8”x12.5”x3.5” with power density above 35W/inch³. Each switch includes two SiC MOSFET C2M0160120D in parallel and output diodes DR1 and DR2 are SiC diode C3D16060D with two in parallel per device.

Figure 6: the prototype picture of 8kW full bridge ZVS LLC resonant converter with 1200V SiC MOS

Figure seven calculates the loss breakdown with 8kW full load at nominal 700V input and 270V output. The left one is based on SiC MOSFET with a proposed two-level full-bridge ZVS resonant converter in figure three and the right one is based on Si MOSFET with three-level converter topology in figure one. The Si MOSFET is based on SPW47N60CFD with two in parallel per switch. From the calculation, even though the resonant frequency with SiC is double at 260 kHz compared with the Si-based solution, the total losses of SiC MOSFET are still 10W lower than the total losses of Si MOSFET. With smaller sized magnetic components, the total solution losses with SiC MOSFET is possible to have losses 20W lower than the Si MOSFET solution. Target efficiency at full load is about 98 percent with SiC MOSFET.

Figure 7: Loss breakdown with SiC MOSFET at fr=260 kHz (left) and Si MOSFET at fr=130 kHz (right)

Operation Waveforms
Figure nine gives the waveforms at full load (8kW) and minimum load (400W) with different input voltages: 650V, 700V and 750Vdc. It includes the waveforms of resonant tank voltage Vab (green) and resonant current Ilr (yellow). At nominal 700V input, the primary current Ilr is a pure sinusoidal waveform with switching frequency fs=fr=260 kHz and it is most optimized performance and efficiency. The minimum switching frequency fs=200 kHz, which occurs at 650V input and the 8kW full load condition and maximum switching frequency fs=410 kHz occurs at 750V input and 400W minimum load. The switching frequency is modulated within 200 kHz to 410 kHz to maintain output at 270V with wide input voltage from 650V to 750V.

Efficiency and Thermal
Figure ten is the measured data for efficiency and thermals. From the efficiency curve, when input voltage is at 700V, the maximum efficiency occurs at 60 percent loading. With 98.3 percent and at full loading the efficiency is 98.1 percent, which is aligned with the loss calculation data in figure seven. At 650V input, because of the circulating conduction losses during t2 to t3 and t5 to t6, the efficiency is lower than 700V input. At 750V input, because of higher switching
frequency and continuous current mode with hard-switching of DR1 and DR2, the efficiency is lower than 700V and 650V. This efficiency test data is the same with loss estimation. The thermal performance is measured at 700V full load 8kW after one hour stable operation. In this test, only one 12W fan is used to cool the transformer T1 and inductor Lr. The heatsink of SiC MOSFET has almost no forced-air moving past it, but the temperature of SiC MOSFET and its heatsink are still within 60°C. The hottest component in the prototype is the transformer T1 and Inductor Lr. The core material of transformer and inductor uses popular low-cost PC95 ferrite, if low-core loss ferrite is used, the temperature of the magnetics is reduced to give much higher overall performance.

**Conclusion**

This paper describes the use of 1200V SiC MOSFETs as a soft-switching resonant converter. A SiC-based 8kW ZVS LLC resonant converter proves SiC MOSFET can innovate to simplify the design of high-voltage input isolated DC/DC converter with high-performance.

To learn more, visit response.cree.com/SiC_RefDesigns to access all of Cree power’s reference designs.

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**Figure 8: Full load waveforms at 8kW** (left: Vin=700V; middle: Vin=650V; right: Vin=750V); (Blue: Vgs_Q3at 10V/div); (Pink: Vgs_Q4at 10V/div); (Yellow: ILrat 10A/div); (Green: Vbat 500V/div)

**Figure 9: Minimum load waveforms at 400W** (left: Vin=700V; middle: Vin=650V; right: Vin=750V); (Blue: Vgs_Q3at 10V/div); (Pink: Vgs_Q4at 10V/div); (Yellow: ILrat 10A/div); (Green: Vbat 500V/div)
Figure 10: Efficiency and thermal performance of 8kW full bridge ZVS LLC resonant converter

References


[4] Jimmy Liu etc, “Increase Efficiency and Lower System Cost with 100 kHz, 10kW Silicon Carbide (SiC) Interleaved Boost Circuit Design,” PCIM Europe 2013, pp. 36-42.