4H-SiC 1200 V Junction Barrier Schottky Diodes with High Avalanche Ruggedness

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Abstract. A state-of-the art family of 1200 V junction barrier Schottky (JBS) diodes was developed. These devices are highly competitive in switching applications thanks to low specific series resistance (1.8 mΩ.cm^2 at current rating) and low capacitive charge (1420 nC.cm^{-2} at 800 V). A uniform avalanche distribution over the active area combined with an optimized high-voltage termination provides industry-leading UIS capabilities. Stringent reliability tests were performed to meet the qualification requirements for the industrial market.

Introduction

Recent improvements in silicon carbide technology drove costs down and made these wide bandgap devices attractive for energy saving in a wide variety of industrial and consumer applications [1,2,3]. SiC Schottky diodes, for example, inserted as free-wheeling diodes could drastically reduce the switching loss of a system [4]. For successful commercialization, device engineers focus on achieving low on-state voltage drop (to minimize the conduction loss) and reducing junction capacitance (to minimize switching loss). High-quality epitaxy provides the opportunity for designs with high avalanche ruggedness, improving the device reliability in the field.

Device Design

Microsemi developed and commercialized a family of 4H-SiC 1200 V Schottky diodes with single die designs for 10, 30, and 50 A. These devices are based on a junction barrier Schottky (JBS) structure with titanium top metal (ΦB≈1.2 eV, Fig. 1). This design scheme allows field-induced barrier lowering to be kept under control, resulting in low leakage currents. TCAD simulations were performed to get insights into the device operation and optimize the design (PITCH1 and PITCH2 on Fig. 1). TCAD results at 1200 V demonstrate an electric field of 1.55E6 V.cm^{-1} near the Schottky barrier, which is significantly lower than the maximum field of 2.55E6 V.cm^{-1} near the PWELL junction.

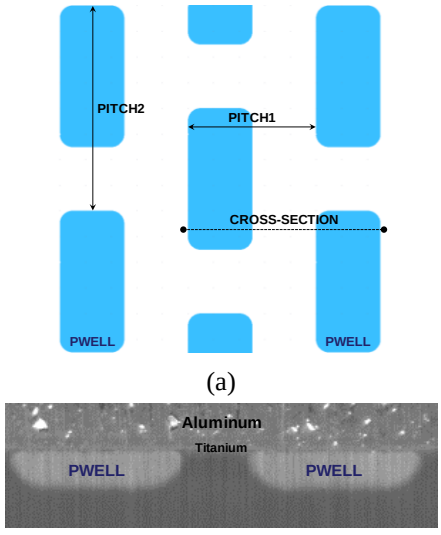
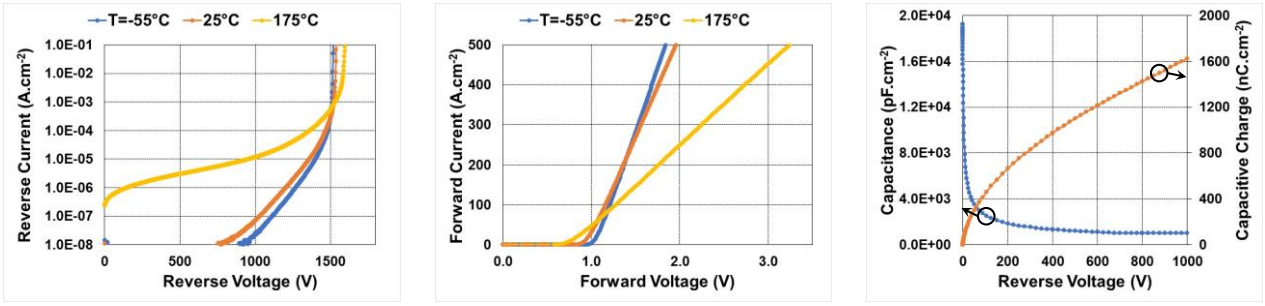


Fig. 1. Layout (a) and SEM cross-section (b) of the 1200 V JBS diode

Characterization

DC and Dynamic Characterization. The 1200 V leakage current densities (per active area) are only 0.9 and 25 µA.cm^{-2} at 25 and 175°C (Fig. 2 a). In the forward mode, the current

density could be as high as 270 A.cm^{-2} to meet a typical 1.5 V target at current rating. The forward voltage at constant current densities increases moderately with temperature, reaching 2.1 V at 175°C (Fig. 2 b). In terms of die size, the 10, 30, and 50 A active area footprints are 0.036, 0.106, and 0.178 cm^2, respectively. The Microsemi (MSC) diodes were benchmarked against those of several leading competitors (COMP. A, B, C) and were shown to have lower specific series resistance (Fig. 3). The dynamic characterization demonstrates a junction capacitance of 1.5E4 pF.cm^{-2} at 1 V and a capacitive charge of 1420 nC.cm^{-2} at 800 V (Fig. 2 c).



(a) (b) (c)

Fig. 2. Reverse IV characteristics (a), forward IV characteristics (b), and reverse CV and Q_C characteristics (c). I, C, and Q_C are normalized per active area.

Avalanche Ruggedness. Further design optimizations were carried out to enable high avalanche ruggedness. This feature provides a competitive advantage for applications prone to unclamped inductive switching (UIS) [5,6]. The PWELL doping profile was engineered to provide a uniform avalanche distribution over the active area. A shallow high-doped implantation was added to make ohmic contacts on the PWELLs, which collect the avalanche current. To avoid early failures in the high-voltage termination, it was designed to reach avalanche breakdown at a higher voltage than the active area. Backside emission microscopy performed with a Hamamatsu Phemos-1000 confirms the whole active area to be in conduction while no current flows in the termination (Fig. 4 a). The 10 A diode was tested for UIS with both 10 and 100 mH inductances. Device failures were reported for energies of 9.8 and 15.5 J.cm^{-2}, respectively. Post-test die inspections show burn marks at random locations in the active area (Fig 4 b, c). UIS tests on parts from other SiC device suppliers (COMP. A, B, C) placed Microsemi's part in a leading position, with energy levels per active area at least 20% above the competition (Fig. 5).

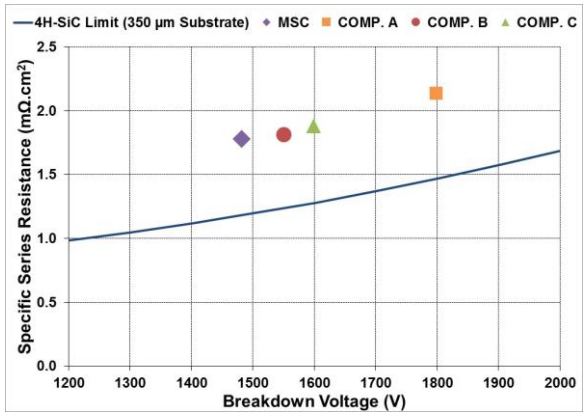
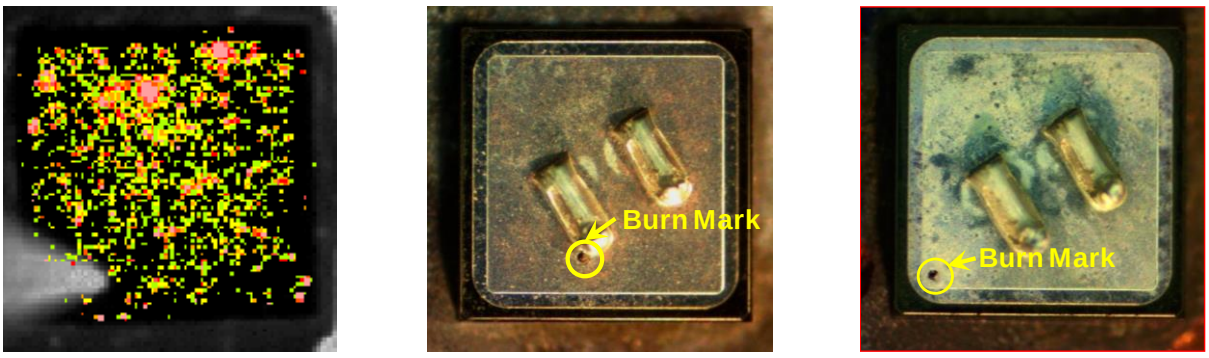


Fig. 3. Specific series resistance versus breakdown voltage for this work (MSC) and leading competitors (COMP. A, B, C)



(a) (b) (c)

Fig. 4. Backside emission imaging at the avalanche onset (a), die inspections post 100 mH (b), and 10 mH (c) failures

TCAD simulations on Synopsys Sentaurus platform were leveraged to get insight into the diode operation during a UIS event. A careful calibration of the thermal effects is required to model the self-heating. This calibration relied on the voltage waveform, as the breakdown voltage increases with the temperature. The maximum voltage increase was matched by tweaking the topside contact thermal resistance (Fig 6). The simulation gives a maximum temperature of 270°C. Importantly, the avalanche carrier generation is along the PWELL planar junction, and there is high heat generation in the epitaxy layer (Fig. 8). When the maximum temperature is reached, the heat does not have the time to diffuse through the 350 µm thick substrate, and the temperature is the highest near the topside contact (Fig. 7). The thermal properties of the topside metal could affect the avalanche ruggedness and possibly provide a knob for further performance improvements.

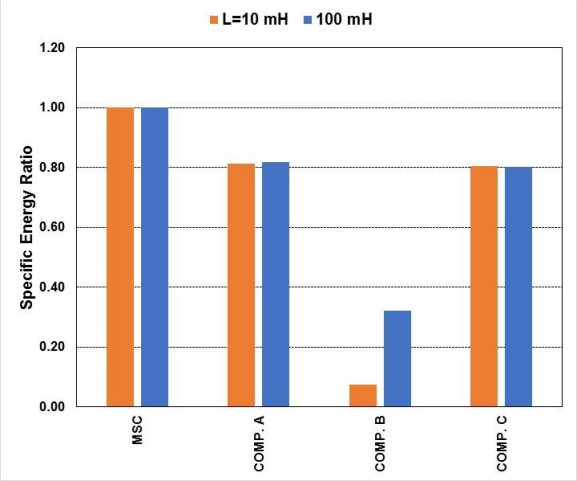


Fig. 5. Specific UIS energy (per active area) before failure normalized to Microsemi diodes results for three leading competitors (COMP. A, B, C)

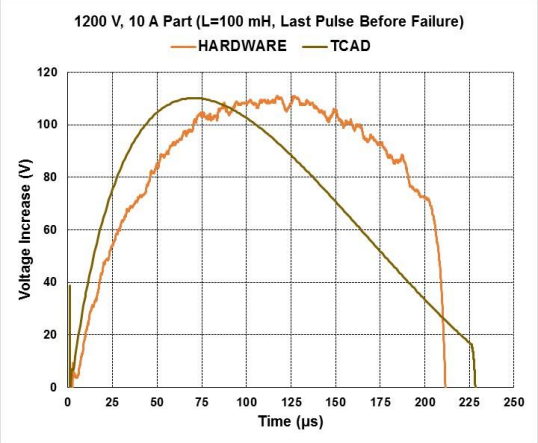


Fig. 6. Breakdown voltage increase during the last pulse before failure

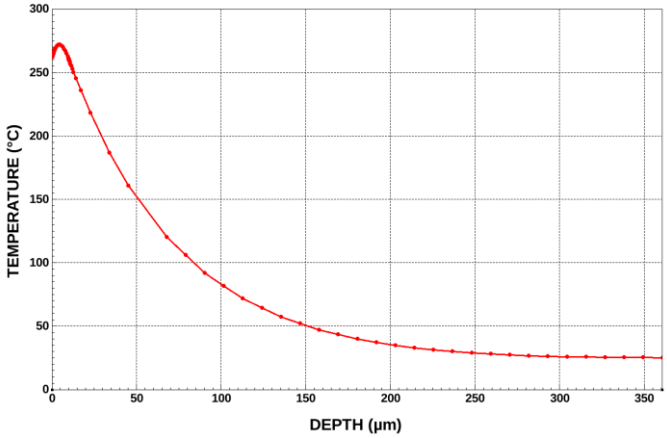


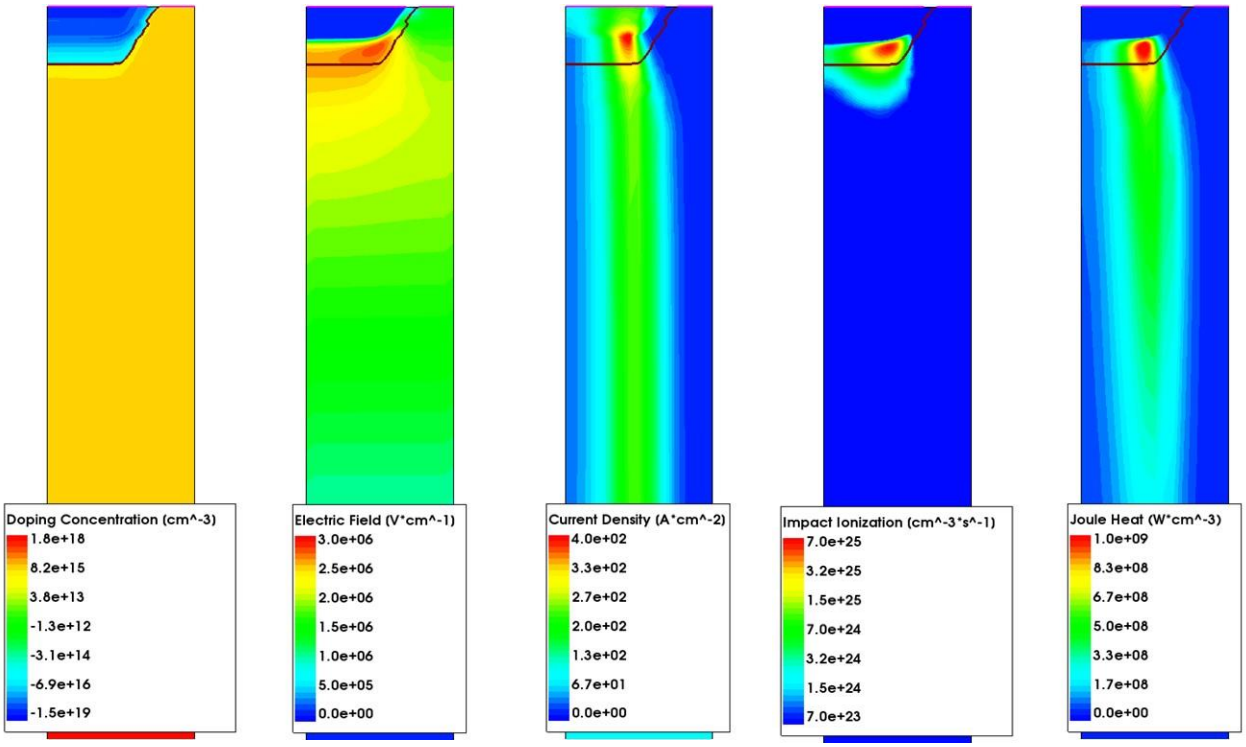
Fig. 7. Vertical temperature profile in the device (t=70 µs)

Repetitive UIS tests were also performed for 10 A and 0.56 J.cm^{-2} pulses with 100 Hz switching frequency. No drift in the electrical parameters was observed after 16 hours.

Reliability Tests. Reliability data were collected as part of the qualification process. No failures were reported after 1000 hours of HTRB stress (960 V, 175°C) and 10,000 power cycles (junction temperature increase of up to 100°C). Qualification under the AEC-Q101 standard targeted for automotive applications is currently ongoing.

Summary

A state-of-the art family of 4H-SiC 1200 V JBS diodes was presented. The forward series resistance at current rating is 1.8 mΩ.cm^2, the leakage current at 1200 V is 0.9 µA.cm^{-2}, and the capacitive charge at 800 V is 1420 nC.cm^{-2}. Industry leading avalanche ruggedness was reported thanks to a design ensuring a uniform breakdown over the active area. The UIS energies at failure for 10 and 100 mH are 9.8 and 15.5 mJ.cm^{-2}, respectively. TCAD simulations of UIS events allowed the extraction of the maximum temperature in the device (270°C). This family of diodes is expected to accelerate the adoption of SiC in the industrial and automotive markets.



(a) (b) (c) (d) (e)

Fig. 8. TCAD results for the doping profile (a), the electric field (b), the current density (c), the impact ionization rate (d), and the heat generation (e) when the temperature maximum is reached at t=70 µs

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