Subminiature, Low-power DACs Address High Channel Density Transmitter Systems

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Introduction

The volume of broadband data transmitted in cable systems has increased tremendously over the last decade. Since 2003, the number of subscribers to broadband data cable services has increased at a compound annual growth rate approaching 14% [1]. The annual growth rate has since slowed, but recent trend information shows double digit growth in premium, so-called "wideband" broadband services.

These services provide higher downstream and upstream bandwidths for heavy data users. The trend of increased data use shows no signs of slowing, as more and more consumers utilize Web-based services for video streaming, audio-streaming, and gaming.

Cable service providers are upgrading their distribution systems to stay ahead of the increased consumer demand for data. The nature of the transmission systems is evolving from a multi-cast system, where all subscribers are sent the same signal, to a combined multi-cast and narrowcast system, where some content is shared by all subscribers, and some content is directed to a particular subscriber. It is the increase in narrowcast services, which includes data but also can include on-demand video, pay-per-view, and other services, that is requiring continued network upgrades.

Cable System Downstream Transmitters

Digital cable transmitters have advanced from a conventional transmitter, where a pair of baseband DACs are used to drive a quadrature modulator, whose local oscillator is used to choose the correct RF frequency, to direct modulation techniques.

In the direct modulation transmitter, an RF DAC is used and the cable channel is created entirely in the digital domain, typically an FPGA. The digital signal is sent from the FPGA to an RF DAC, where it is converted to an analog signal and sent to the power amplifier. A simplified block diagram of a typical cable transmitter is shown in Figure 1.
Figure 1. Block diagram of (a) typical cable transmitter using multiple RF DACs and an RF combiner to achieve a full cable spectrum, and (b) a new cable transmitter using the new AD9129 RF DAC.

In Figure 1(a), the transmitter is composed of several RF DACs being driven by several FPGAs, and then the output of each of the RF DACs is sent to a pre-amplifier. The outputs of the pre-amplifiers are combined to feed into a single power amplifier which drives the cable plant.

This architecture is used because the gate count and capacity of the FPGAs to synthesize large numbers of digital signals with a reasonable current consumption was limited, and each RF chain could be optimized for a particular frequency band.

The RF DACs often have signal processing on them that limit the total RF bandwidth that can be generated, but ease the interface requirements for the FPGAs. Previous generation RF DACs had good performance, but harmonic performance did not meet the demanding DOCSIS specifications, so detailed frequency planning and RF filter design was necessary to achieve acceptable performance.

The architecture, which may have two, four, or eight 256-QAM channels per RF DAC, allows for scalability, albeit at a cost of extra hardware. There are several disadvantages to it. The RF combiner gets more complicated with a higher number of channels desired, and with each added DAC channel, the combiner’s losses also increase.

Each of the FPGA+RF DAC+pre-amplifier chains draws a significant amount of power, maybe 10 Watts per channel. The multiple RF chains needed could require multiple cards to achieve a 158-channel, full cable spectrum, with each card...
drawing as much as a kilowatt or more. Housing multiple cards in a single facility is necessary to service an example 1000 household group.

The system becomes big, with many cards needed to serve each 1000 household group. The result is a need for a large facility or building to house all of these cards in large racks or chassis, with significant attention paid to cooling systems for the racks, and expenses are high to keep the building at a reasonable operating temperature.

Today, with the higher gate counts and finer-line CMOS processes available, it is possible for FPGAs to have high enough density to enable creation of the entire 158 6 MHz-wide cable channels on one FPGA, driving one RF DAC. When combined with the new AD9129 RF DAC from Analog Devices, a much simplified cable transmitter can be designed.

Figure 1(b) shows a block diagram of a new transmitter that is capable of synthesizing the entire downstream cable spectrum from 50 MHz to 1 GHz. The digital modulator in the FPGA drives the AD9129 RF DAC with a high sample rate of up to 2.8 GSPS.

The DAC has an optional 2x interpolator filter that can be enabled to implement on-chip digital filtering for out-of-band components, which increases the effective sampling rate to up to 5.6 GSPS. The DAC output is filtered with a low pass filter and sent to a new, highly integrated variable gain amplifier and driver amplifier from TriQuint, the TAT2814.

The amplifier achieves new levels of integration by integrating a pre-amplifier, a variable attenuator, and a driver amplifier all in a single module. This enables a compact layout for the radio section and reduces the physical size of each radio port.

Example Design

RF DAC

The AD9129 RF DAC is sampled at rates as high as 2.8 GSPS. The advantage of such a high sampling rate is that the DAC images are folded around a higher $f_{DAC}/2$ than previous solutions. This prevents the images from folding below 600 MHz, easing the requirements for their suppression. The data is transferred into the DAC via a dual LVDS port clocked at up to 700 MHz, with data being clocked in on both edges of the clock for a 1.4 GHz data transfer rate over each port.

The current-steering architecture [3] and careful design of the DAC enable superior spurious performance and a low noise floor. The DAC is implemented in a 0.18 µm CMOS process, giving low power consumption of about 1.1W.

Low Pass Filter
Between the DAC and amplifier, passive signal conditioning can help meet DOCSIS specifications for out of band rejection and power variation across the cable band. In the example design, a 7th order elliptical filter was chosen to address the issue of out of band rejection. The AD9129 DAC’s lower sample rate of 2.305 GSPS was used in evaluation of the low pass filters out of band performance, since the images fold closer to the cable band with the lower sample rate.

The image for a 1 GHz channel was of particular concern, since it lands at 1.3 GHz, only 300 MHz away from the desired signal. The design achieved 62.5 dBC of image rejection for the 1.3 GHz image, meeting the DOCSIS specification for out of band rejection.

Two series resonant equalizer tanks were used to address the issue of power variation across the cable band due to the sinc rolloff at the output of the DAC and additional rolloff in the power amplifier. The equalizers achieved a power variation of about 1.4 dB between the highest power channel and lowest power channel in the band, meeting DOCSIS specs without any digital manipulation of the input signal. The power of each individual channel can be adjusted digitally to achieve a finer tuned flatness across the band.

**Output Amplifier**

The TAT2814 output amplifier combines three functions into a single package, greatly reducing board space with the high level of integration. The amplifier delivers a total possible gain of about 30 dB. The output is capable of delivering up to +65 dBmV of power for a 1-channel 256-QAM signal. The amplifier is implemented in a GaAs process and is optimized for low power operation. The total power consumption of the integrated device is about 4.2W.

**Non-Linear Correction**

Non-Linear Correction (NLC) is used to improve the in band harmonic performance of the full signal chain, correcting distortion that comes from the DAC as well as from the power amplifier and any other distortion which may occur along the signal chain. The NLC process can be programmed to bring the board to meet specifications, or to allow for a specified margin to allow for manufacturing tolerances. NLC calibration only takes minutes and can greatly improve a system’s performance.

**Measured Results**

A board was designed with the AD9129 in an optimized layout, and its performance was measured. (See Image 1, below.) A signal with all 158 channels was used to test the flatness of the board’s response across the cable band. Figure 2 shows the optimized board’s output with the full band signal as the input. The power variation between the highest and lowest power channels is only about 1.4 dB, within the DOCSIS specifications and can be further improved with digital manipulation of the input signal.
Image 1. Board designed with the AD9129 in an optimized layout
Tests show that boards can be reliably corrected with 4 dB of margin, making the system robust against manufacturing tolerances. Figure 3 and Figure 4 shows the performance of the second and third harmonic with NLC for 4 carriers. In the plots, the blue line represents the DOCSIS specifications. The data was taken with 2304 MHz as the DAC update rate.
Figure 3. Four Carrier Second Harmonic Performance with NLC

Figure 4. Four Carrier Third Harmonic Performance with NLC
Conclusions

Cable systems are being upgraded to support the rapid increase in demand for data services, and reduced space and power consumption are key drivers for new designs to accommodate more channels. RF DACs such as the AD9129 are enabling equipment suppliers to achieve new levels of channel density while delivering smaller size and lower power consumption.

References


About the authors

Daniel E. Fague is the Applications Engineering Manager in the high speed digital-to-analog converters group at Analog Devices. He received his BSEE from Gonzaga University in 1989 and his MSEE from the University of California at Davis in 1991. He joined Analog Devices’ wireless handset group in 1995 where he focused on handset radio architecture design, including direct conversion radios, for GSM, EDGE, CDMA, and Bluetooth. Prior to that, he worked for 5 years at National Semiconductor doing radio architecture design for DECT and PHS. He holds 7 patents and has published more than 30 articles and papers.

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