34-44GHz Low Noise Amplifier
GaAs Monolithic Microwave IC

Description
The CHA2494-98F is a wide band monolithic low noise amplifier. It is designed for a wide range of applications, from military to commercial communication systems. The circuit is manufactured with a pHEMT process, 0.15µm gate length, via holes through the substrate, air bridges and electron beam gate lithography. It is available in chip form.

Main Features
- Broadband performances: 34-44GHz
- 3dB noise figure
- 20dB gain
- 20dBm Output IP3
- DC bias: Vd=4V @ Id=80mA
- Chip size 2.59x1.16x0.1mm

Main Electrical Characteristics
Tamb.= +25°C

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Freq</td>
<td>Frequency range</td>
<td>34</td>
<td>44</td>
<td></td>
<td>GHz</td>
</tr>
<tr>
<td>Gain</td>
<td>Linear Gain</td>
<td>20</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>NF</td>
<td>Noise Figure</td>
<td>3.0</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>OIP3</td>
<td>3rd order intercept point</td>
<td>20</td>
<td></td>
<td></td>
<td>dBm</td>
</tr>
</tbody>
</table>
Electrical Characteristics

Tamb. = +25°C, Vd = +4V

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Freq</td>
<td>Frequency range</td>
<td>34</td>
<td>44</td>
<td>GHz</td>
<td></td>
</tr>
<tr>
<td>Gain</td>
<td>Linear Gain</td>
<td>20</td>
<td></td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>NF</td>
<td>Noise Figure</td>
<td>3.0</td>
<td></td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>RLlin</td>
<td>Input Return Loss</td>
<td>-8</td>
<td></td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>ROut</td>
<td>Output Return Loss</td>
<td>-8</td>
<td></td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>OIP3</td>
<td>Output 3rd order intercept point</td>
<td>20</td>
<td></td>
<td>dBm</td>
<td></td>
</tr>
<tr>
<td>OP1dB</td>
<td>Output Power @1dB comp.</td>
<td>12</td>
<td></td>
<td>dBm</td>
<td></td>
</tr>
<tr>
<td>Vg</td>
<td>Gate voltage</td>
<td>-0.45</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Id</td>
<td>Drain current</td>
<td>80</td>
<td></td>
<td>mA</td>
<td></td>
</tr>
</tbody>
</table>

These values are representative of on-wafer measurements that are made without bonding wires at the RF ports.
A bonding wire of typically 0.3 to 0.4nH will improve the matching at the accesses.

Absolute Maximum Ratings (1)

Tamb. = +25°C

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Values</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vd</td>
<td>Drain bias voltage</td>
<td>4.5V</td>
<td>V</td>
</tr>
<tr>
<td>Id</td>
<td>Drain bias current</td>
<td>160</td>
<td>mA</td>
</tr>
<tr>
<td>Vg</td>
<td>Gate bias voltage</td>
<td>-2 to +0.4</td>
<td>V</td>
</tr>
<tr>
<td>Tj</td>
<td>Junction temperature</td>
<td>175</td>
<td>°C</td>
</tr>
<tr>
<td>Ta</td>
<td>Operating temperature range</td>
<td>-40 to +85</td>
<td>°C</td>
</tr>
<tr>
<td>Tstg</td>
<td>Storage temperature range</td>
<td>-55 to +150</td>
<td>°C</td>
</tr>
</tbody>
</table>

(1) Operation of this device above any one of these parameters may cause permanent damage.

Typical Bias Conditions

Tamb. = +25°C

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Values</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vd</td>
<td>DC drain voltage</td>
<td>4</td>
<td>V</td>
</tr>
<tr>
<td>Id</td>
<td>DC drain current controlled with Vg</td>
<td>80</td>
<td>mA</td>
</tr>
<tr>
<td>Vg</td>
<td>DC gate voltage</td>
<td>-0.45</td>
<td>V</td>
</tr>
</tbody>
</table>
Typical on wafer Measurements

Tamb = +25°C, Vd = +4V, Id = 80mA

Sij parameters

Noise figure
Typical Test Fixture Measurements

Tamb = +25°C, Vd = +4V, Id = 80mA

**Gain versus frequency & temperature**

*Graph showing gain in dB versus frequency and temperature for +25°C, -40°C, and +85°C.*

**Return loss versus frequency**

*Graph showing return loss in dB versus frequency for input and output return loss.*
Typical Test Fixture Measurements

$\text{Tamb} = +25°C, \ Vd = +4V, \ Id = 80mA$

**Noise figure versus frequency & temperature**

-40°C  
+25°C  
+85°C

**Output Power @ 1dB comp. versus temperature at 80mA**

25°C  
-40°C  
+85°C

**Output Power @ 1dB comp. versus temperature at 120mA**

25°C  
-40°C  
+85°C
Typical Test Fixture Measurements

Tamb = +25°C, Vd = +4V, Id = 80mA

Output IP3 versus frequency at 80mA

Output IP3 versus frequency at 120mA

Output IP3 versus temperature at 80mA & 40GHz

Output IP3 versus temperature at 120mA & 40GHz

Linear gain versus current
Mechanical data

Note: Supply feed should be bypassed. 25µm diameter gold wire is to be preferred.

Chip thickness: 100µm
DC pad size: 86x83µm
RF pad size: 105x172µm

Chip size: 2590x1160 ±35µm
All dimensions are in micrometers
Recommended assembly plan

Note: Supply feed should be bypassed. 25µm diameter gold wire is to be preferred.

Recommended circuit bonding table

<table>
<thead>
<tr>
<th>Label</th>
<th>Type</th>
<th>Decoupling</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>VD</td>
<td>Vd</td>
<td>120pF</td>
<td>Drain Supply</td>
</tr>
<tr>
<td>VG</td>
<td>Vg</td>
<td>120pF</td>
<td>Gate Supply</td>
</tr>
</tbody>
</table>
Evaluation mother board

- Based on typically Ro4003 / 8mils or equivalent.
- Decoupling capacitors of 120pF are recommended for all DC accesses.
- The board losses are estimated from 2 to 3dB in the frequency range.
DC Schematic

LNA: 4V, 80mA

Vd = 4V

Vg # -0.45V

Ref. : DSCHA24941144 - 24 May 11

Specifications subject to change without notice

Route Départementale 128, BP46 - 91401 ORSAY Cedex - FRANCE
Tel.: +33 (0) 1 69 33 03 08 - Fax: +33 (0) 1 69 33 03 09
Notes

Due to ESD protection circuits on RF input and output, an external capacitance might be requested to isolate the product from external voltage that could be present on the RF accesses.

![Diagram of the amplifier circuit]

ESD protections is also implemented on gate access common to 3rd and 4th stage (1st and 2nd stage are self-biased).

Due to BCB coating on the chip, qualification domain implies the chip must be glued.

Biasing conditions:

Vg could be tuned to reach 120mA in order to increase the output power and the gain (see pages 5 & 6).

The current has no influence on Noise figure.
Recommended ESD management

Refer to the application note AN0020 available at http://www.ums-gaas.com for ESD sensitivity and handling recommendations for the UMS package products.

Ordering Information

Chip form: CHA2494-98F/00

Information furnished is believed to be accurate and reliable. However United Monolithic Semiconductors S.A.S. assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of United Monolithic Semiconductors S.A.S.. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. United Monolithic Semiconductors S.A.S. products are not authorised for use as critical components in life support devices or systems without express written approval from United Monolithic Semiconductors S.A.S.