55-65GHz Self biased Single Side Band Mixer

GaAs Monolithic Microwave IC

Description

The CHM1298 is a multifunction chip (MFC) which integrates a LO buffer amplifier and a sub-harmonically balanced diode mixer for 2LO suppression and image rejection. It is usable both for up-conversion and down-conversion. It is designed for a wide range of applications, from military to commercial communication systems. The backside of the chip is both RF and DC grounded. This helps to simplify the assembly process.

The circuit is manufactured with a pHEMT process, 0.25µm gate length, via holes through the substrate, air bridges and electron beam gate lithography.

It is available in chip form.

Main Features

- Broadband performance: 55-65GHz
- 12dB conversion Loss
- 10dBc image rejection
- +10dBm LO input power
- +0dBm input power (1dB gain comp.)
- DC power consumption: 90mA @ 3.5V
- Chip size: 2.10x1.17x0.10mm

Main Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>FRF</td>
<td>RF frequency range</td>
<td>55</td>
<td>65</td>
<td>GHz</td>
<td></td>
</tr>
<tr>
<td>FLO</td>
<td>LO frequency range</td>
<td>27.5</td>
<td>32.5</td>
<td>GHz</td>
<td></td>
</tr>
<tr>
<td>FIF</td>
<td>IF frequency range</td>
<td>DC</td>
<td>5</td>
<td>GHz</td>
<td></td>
</tr>
<tr>
<td>Lc</td>
<td>Conversion Loss</td>
<td>12</td>
<td>dB</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

ESD Protection: Electrostatic discharge sensitive device. Observe handling precautions!
Electrical Characteristics for Broadband Operation

\( \text{Tamb} = +25^\circ \text{C} \)

<table>
<thead>
<tr>
<th>Symbol</th>
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<td>Lc</td>
<td>Conversion Loss</td>
<td>12</td>
<td>dB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PLO</td>
<td>LO Input power</td>
<td>+10</td>
<td>dBm</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2xLO Leak</td>
<td>2xLO Leakage (for PLO = +5dBm)</td>
<td>-35</td>
<td>dBm</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Img Rej</td>
<td>Image Rejection (^{(1)})</td>
<td>10</td>
<td>dBc</td>
<td></td>
<td></td>
</tr>
<tr>
<td>P1dB</td>
<td>Input power at 1dB gain compression</td>
<td>+0</td>
<td>dBm</td>
<td></td>
<td></td>
</tr>
<tr>
<td>P03</td>
<td>Input power at 3dB gain compression</td>
<td>+2</td>
<td>dBm</td>
<td></td>
<td></td>
</tr>
<tr>
<td>IP3</td>
<td>Input 3rd order intercept point</td>
<td>+8</td>
<td>dBm</td>
<td></td>
<td></td>
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<tr>
<td>LO Match</td>
<td>LO Matching</td>
<td>2.0:1</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>RF Match</td>
<td>RF Matching</td>
<td>2.0:1</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>IF Match</td>
<td>IF Matching</td>
<td>2.0:1</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Id</td>
<td>Bias current</td>
<td>90</td>
<td>mA</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

\(^{(1)}\) With external quadrature hybrid coupler (reference on request). The minimal value depends on the quality of the external quadrature combiner.

* A bonding wire of typically 0.1 to 0.15nH will improve the accesses matching.

Absolute Maximum Ratings

\( \text{Tamb} = +25^\circ \text{C} \) \(^{(1)}\)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Values</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vd</td>
<td>Drain bias voltage</td>
<td>4.0</td>
<td>V</td>
</tr>
<tr>
<td>Id</td>
<td>Drain bias current</td>
<td>150</td>
<td>mA</td>
</tr>
<tr>
<td>P_{LO}</td>
<td>Maximum LO input power</td>
<td>15</td>
<td>dBm</td>
</tr>
<tr>
<td>Ta</td>
<td>Operating temperature range</td>
<td>-40 to +85</td>
<td>°C</td>
</tr>
<tr>
<td>Tstg</td>
<td>Storage temperature range</td>
<td>-55 to +125</td>
<td>°C</td>
</tr>
</tbody>
</table>

\(^{(1)}\) Operation of this device above anyone of these parameters may cause permanent damage.
Typical On-wafer Measurements in Up-Conversion mode with external combiner
Bias conditions: Tamb=+25°C, Vd=3.5V, Id=90mA

Up-Conversion mode with external combiner
P LO = +10dBm F IF = 1.0GHz

LO Frequency (GHz) vs.
-44 -40 -36 -32 -28 -24 -20 -16 -12 -8 -4 0

Conversion Losses & 2xLO leakage (dB & dBm)

Pout 2xLO
CL inf
CL sup

Up-Conversion mode with external combiner
P LO = +10dBm F IF = 2.0GHz

LO Frequency (GHz) vs.
-44 -40 -36 -32 -28 -24 -20 -16 -12 -8 -4 0

Conversion Losses & 2xLO leakage (dB & dBm)

Pout 2xLO
CL inf
CL sup

Up-Conversion Sup. compression with external combiner
LO = 30GHz P LO = +10dBm IF = 2.0GHz (RF = 62GHz)

LO Frequency (GHz) vs.
-15 -13 -11 -9 -7 -5 -3 -1

Output power & Conv. Losses (dBm & dB)

Pout Sup I
Pout Inf Q
CL Sup I
CL Inf Q

Up-Conversion Inf. compression with external combiner
LO = 30GHz P LO = +10dBm IF = 2.0GHz (RF = 58GHz)

LO Frequency (GHz) vs.
-15 -13 -11 -9 -7 -5 -3 -1

Output power & Conv. Losses (dBm & dB)

Pout Inf I
Pout Sup Q
CL Inf I
CL Sup Q
Typical On-wafer Measurements in Down-Conversion mode with external combiner
Bias conditions: Tamb=+25°C, Vd=3.5V, Id=90mA

![Graph showing down-conversion measurements with external combiner]

Typical On-wafer Measurements in Up-Conversion mode without external combiner
Bias conditions: Tamb=+25°C, Vd=3.5V, Id=90mA

![Graph showing up-conversion measurements without external combiner]
Chip Assembly and Mechanical Data

Note: Supply feed should be bypassed. 25µm diameter gold wire is to be preferred. It is necessary to use an external hybrid quadrature combiner on the IF ports if the image rejection functionality is required.

Bonding pad positions.
(Chip thickness: 100µm. All dimensions are in micrometers)
Recommended ESD management

Refer to the application note AN0020 available at http://www.ums-gaas.com for ESD sensitivity and handling recommendations for the UMS products.

Ordering Information

Chip form: CHM1298-99F/00

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