Gallium Nitride RF Technology Advances and Applications

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Gallium Nitride RF Technology Advances and Applications

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***Abstract*—Over the last decade, Gallium Nitride (GaN) proponents have touted the technology as the future for high power cellular base stations that will displace silicon LDMOS devices. One may speculate on how LDMOS technological advances, GaN market acceptance, reliability, or cost have moderated GaN's advance into the LDMOS domain. This paper discusses GaN technology, 200W packaged device performance, a 2.6-2.7 GHz, 400 W Doherty power amplifier, thermal management, and cost vs. performance. It emphasizes how GaN and LDMOS technology complement each other for RF applications. GaN devices have size and performance advantages over Si-LDMOS for frequencies above 2.5 GHz. On the other hand, LDMOS devices perform very competitively at 2.6 GHz using multiple devices in larger size circuits. Unlike Doherty amplifiers where GaN versus Si LDMOS may be a close question, GaN will dominate power amplifiers at frequencies in excess of 3 GHz as well for high efficiency and wideband power amplifiers.**

***Index Terms*—GaN, SiC, Power Amplifier**

I. Introduction

Gallium nitride device technology has been the focus of intense development in the commercial space for the last decade. The advantages of AlGaN/GaN HFET's for RF applications arise from the GaN's high breakdown field strength and high electron sheet density. Table 1 compares the electronic and thermal properties of GaN to Si and GaAs. As seen from the table, GaN has a much higher breakdown field strength than GaAs or Si. These electronic properties allow GaN devices to operate at higher bias voltages and current densities than GaAs or Si devices. This combination of high voltage and high current capability provides for 3-5X higher microwave power density than GaAs and Si technology. The higher power density translates into a smaller device needed for a given output power and a higher watts per unit input and output capacitance. The high thermal conductivity of SiC substrates (4W/cm-K) works with the high power density of the GaN channel material allowing a high degree of heat removal. These electrical and thermal advantages of GaN on SiC compared to GaAs or Si enable high power, wide bandwidth amplifiers that cannot be realized with these competing technologies. In spite of these inherent advantages for GaN, Si-LDMOS continues to dominate the market for RF power transistors. This paper details the technology, RF applications, thermal performance, cost considerations, and future applications of AlGaN/GaN HFET's.

Table 1: Comparison of GaN, Si, and SiC electronic and thermal properties.

Material	GaN	Si	GaAs	SiC (4H)
Bandgap (eV)	3.4	1.1	1.4	3.2
Breakdown Field Strength (MV/cm)	2	0.3	0.4	2.2
Saturated Velocity (x10^7 cm/s)	2.5	1	1.5	2
Johnson Figure of Merit, $E_{br}*v_{sat}/2\pi$ (V/s)	8×10^{12}	0.5×10^{12}	1×10^{12}	7×10^{12}
Thermal Conductivity (W/cm-K)	1.5	1.3	0.4	4

II. GaN and Si-LDMOS Compliment Each Other

In contrast to the view that GaN will be used at the expense of LDMOS devices, the technologies actually complement each other for RF applications. Figure 1 shows published data for power versus frequency showing Si-LDMOS output powers in excess of 1 kW for frequencies of 1 GHz. However, beyond 1.5 GHz, the output impedances for LDMOS devices become more difficult to match.

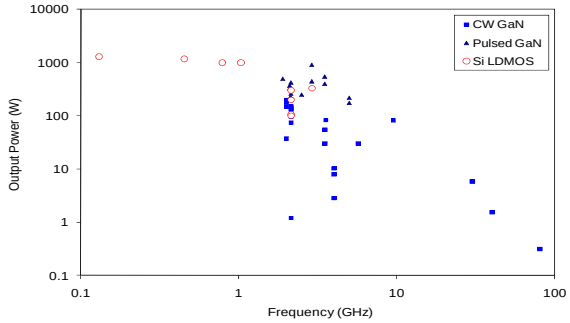

Figure 1: Output power versus frequency for GaN and Si LDMOS devices.

As a result, the achievable output power drops from the kilowatt level to the hundreds of watts level at 2-2.5 GHz. On the other hand, GaN devices have much higher power density

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and output impedances; the drop in achievable pulsed output power does not occur until 4-5 GHz. Because of its performance and cost, LDMOS is very attractive at 2.5 GHz and below. GaN is attractive at 2 GHz and above, where its cost can be justified. Above 3 GHz GaN is the clear winner for powers >10W. Below 2 GHz cost becomes an issue for GaN in narrow band applications. In between 2 and 2.5 GHz performance and cost targets must be considered together.

III. Gallium Nitride Device Technology

The GaN epitaxial wafers used to fabricate the devices presented in this paper were grown on SiC substrates using metal organic chemical vapor deposition. Device structures were fabricated using Freescale's 48V GaN on SiC technology as depicted in Figure 2. The technology includes device isolation, Ti-Al based ohmic contacts, 0.6 µm gates, SiN-based passivation, a source connected field plate, and plated Au airbridges. Ohmic contact resistances are typically 0.2-0.3 Ω-mm. After front side processing, the device wafers were thinned to a thickness of 3 mils and source vias were etched through the SiC substrate and GaN buffer layer. In addition, 10 µm thick plated Au was deposited on the backs of the wafers. Figure 3 shows a picture of a finished 37.8 mm die.

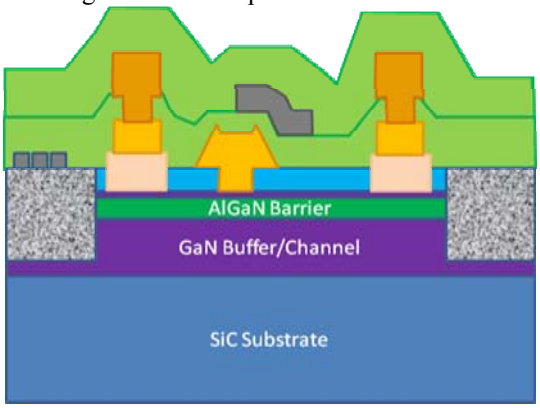

Figure 2: Schematic cross section of GaN HFET device.

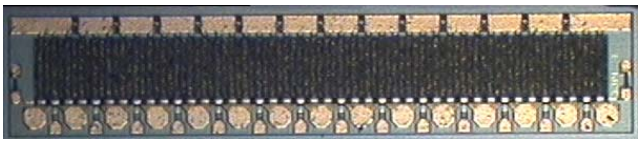

Figure 3: Die photo of a 37.8 mm GaN HFET die. Chip size is 4.7 x 1 mm^2.

As seen from Figure 4, DC and pulsed IV currents show excellent agreement; this indicates very low trapping effects. The maximum drain current of these devices is typically 800 mA/mm. Figure 5 shows that the off-state breakdown voltage is over 200 V for a 0.15 mm device; 200 W devices with 37.8 mm periphery scale to ~150V breakdown voltage because of material defects.

Figure 6 shows the capacitance characteristics for a GaN HFET device. The data show a gate-source capacitance of approximately 2.3 pF/mm, a gate drain capacitance of 0.08 pF/mm, and a drain source capacitance of approximately 0.4 pF/mm at a drain bias of 48V and a drain current of 40 mA/mm (class A-B bias).

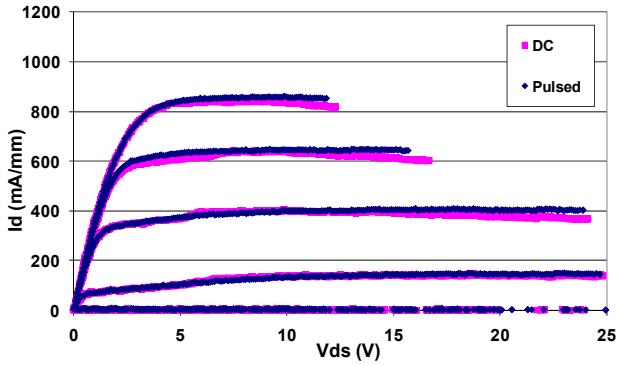

Figure 4: Comparison of DC and pulsed IV curves for 0.3 mm GaN HFET measured at a 10 W/mm power compliance at V_{DS}=0-20V, V_{GS} =-5V to +1V in 1 V steps.

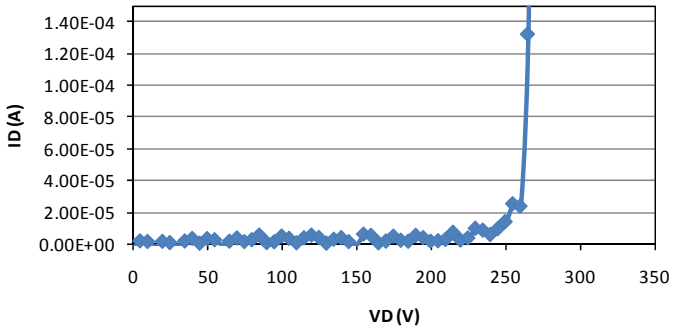

Figure 5: Small-device off-state breakdown characteristics for 0.15 mm GaN HFET device biased at V_{GS}=-5V.

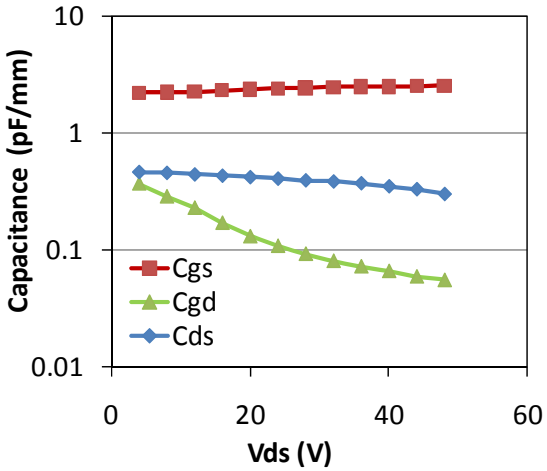

Figure 6: Small-signal capacitance versus drain bias characteristics of a 0.3 mm GaN HFET device biased at a quiescent current of 40 mA/mm.

IV. Characteristics of Internally Matched Devices

After die fabrication and screening, 37.8 mm die were packaged in industry standard NI-780 packages using input matching structures designed based on S-parameters and

loadpull data taken on unit cell devices. The matching structures use series bondwire inductance and shunt MOS-cap capacitance to transform the Z_{in} of the die to greater than 3 ohms for a 200 W device.

The devices of Figure 7 (a) at 2.14 GHz were characterized using a loadpull system configured for pulsed RF excitation. For these tests, the pulse length was 10 μS and the duty cycle was 10%. Figure 9 shows the device performance in both class A-B and Class C operation.

(a) (b)

Figure 7: Photograph of (a) single and (b) dual path packaged transistors using NI-780 package footprints.

The devices of Figure 7(a) were biased at a class A-B quiescent drain bias of 25 mA/mm. At P_{3dB}, they produced >200 W output power and approximately 75% drain efficiency with 17 dB gain. These data are depicted in Figure 8. In class C, the devices were biased at -3.5 V, approximately 0.5 V below pinch-off. Here they had reduced gain, especially at low drive levels, but the P_{3dB} efficiency increased to 78% at P_{3dB} as shown in Figure 9.

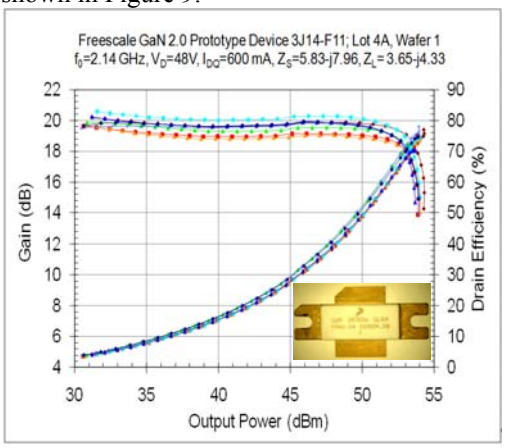

Figure 8: Saturation characteristics over power for a single 37.8 mm die in a NI-780-2 package under 2.14 GHz, 48V pulsed RF conditions in class A-B (600 mA I_{DQ}) operation.

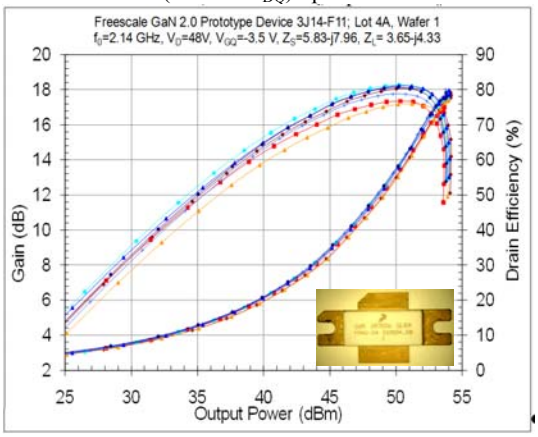

Figure 9: Saturation characteristics over power for a single 37.8 mm die in a NI-780-2 package under 2.14 GHz, 48V pulsed RF class C operation. Device is biased at -3.5 V (0.5 V below threshold).

The dual path packages of Figure 7(b) were built and characterized using a multi-section pre-match. Figure 10 shows the over-frequency power results for these devices at P_{3dB}. Here the output power at P_{3dB} was 300W at 2.1 GHz and 280W at 2.7 GHz. Meanwhile the efficiency was approximately 67% at 2.1 GHz, then leveled off to 63% and then peaks back up to 69% at 2.7 GHz. The frequency dependence of the efficiency comes as a result of the change in harmonic loading as a function of frequency.

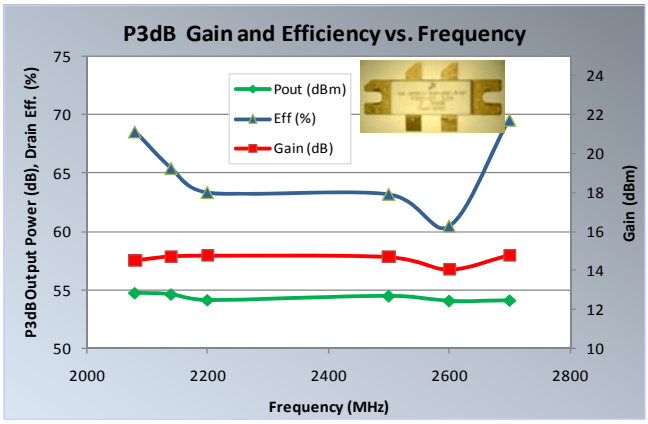

Figure 10: Over-frequency characteristics at P_{3dB} for a single 37.8 mm die in one path of an NI-780-4 package under 2.14 GHz, 48V pulsed RF conditions in (a) class A-B (600 mA IDQ) and (b) class C operation.

V. Characteristics of a 2.6-2.7 GHz 400 W Doherty Power Amplifier

Using the dual path devices of Figure 7(b), were used to realize a 2.6-2.7 GHz Doherty amplifier. Figure 11 shows a photograph of the finished amplifier. The amplifier design takes advantage of the dual path device and uses a very compact layout with an effective area of 8 in^2. For this design, the class AB main amplifier connects directly to the summing node while a quarter-wave transmission line connects the class C main amplifier to the summing node and impedance inverter.

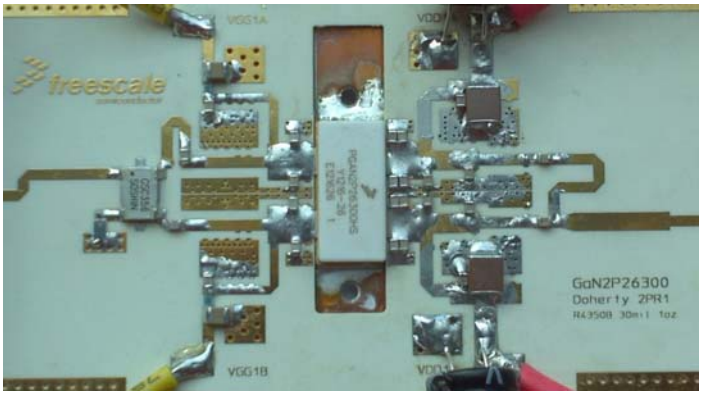

Figure 11: Realized 400 W GaN inverted Doherty PA using single dual path device. Effective circuit area is 2.4" X 3.4" (8 in^2).

Figure 12 shows the measured small signal performance of the finished amplifier showing a small signal gain of 16 dB flatness of 0.43 dB over the 2.6-2.7 GHz LTE band. The 2.69 GHz measured performance at 80 W average power showed a drain efficiency of approximately 45% at a PAR of 7 dB, as shown in Figure 13. The gain was 14 dB at this point. Figure 14 shows that the ACP dropped from -28 dBc to -55 dBc, a correction of 27 dB when tested using digital pre-distortion (DPD) with the same 2-WCDMA signal, at the 80 W condition of Figure 13.

Table 2 compares the performance of the amplifier of Figure 11 with other reported results. As seen from the table, this Doherty amplifier has similar gain and efficiency as compared to others at the 400 W power level. It is worth noting that LDMOS performance is similar, although here it required three discrete devices and a circuit area about 3times larger. If the LDMOS circuit layout were optimized, it would still be approximately two times larger.

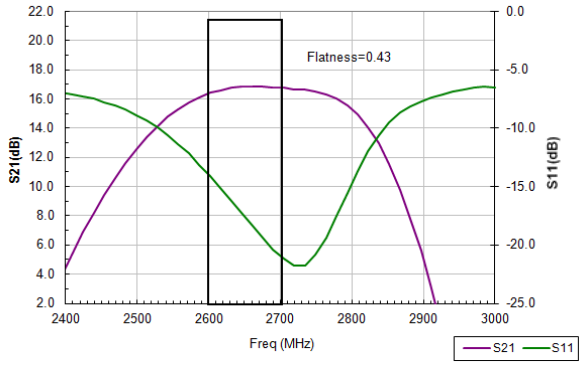

Figure 12: Graph showing measured S21 and S11 for Doherty power amplifier of Figure 11.

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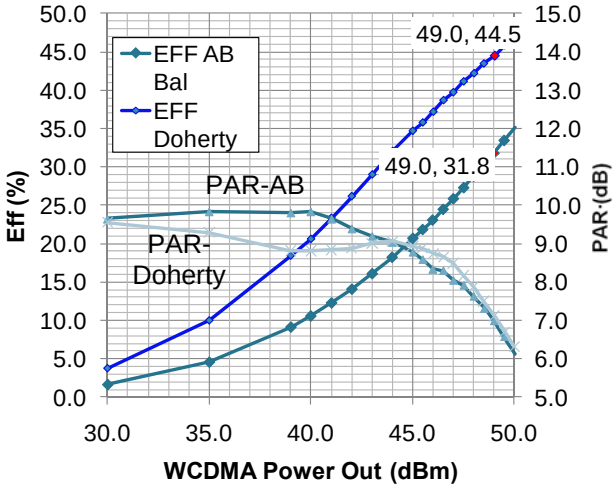

Figure 13: Graph showing output Doherty performance for amplifier of Fig. 5 measured under 2-WCDMA conditions at 2.69 GHz with a 10 dB PAR signal.

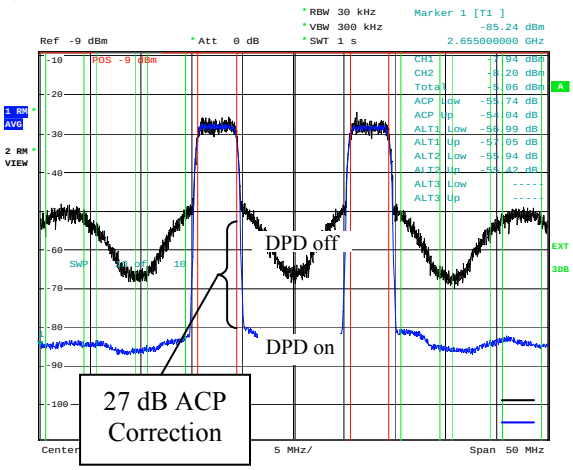

Figure 14: Graph showing Doherty amplifier performance with and without DPD applied for 10 dB PAR, 2.69 GHz W-CDMA signal at 80W average output power, 44.5% drain efficiency.

Table 2: Comparison of reported 2.6-2.7 GHz W-CDMA Doherty Performance.

Technology/ Reference	Peak Power (W)	Drain Eff. (%)	Gain (dB)	Est. Area (in^2)	Signal /PAR	DPD ACP (dBc)
GaN Symmetric [1]	130	47	12	10	WCDMA/ 7.5 dB	-57
GaN 3:2 Asymmetric [2]	530	48	12.5	14	4-WCDMA/ 6.2 dB	-50.6
GaN Symmetric (This Work)	400	44.5	14	8	2-WCDMA 7 dB	-55
LDMOS 2:1 Asymmetric [3]	550	45	13.5	25	2-WCDMA 7 dB	-57

VI. Thermal Management

Thermal management of RF power devices plays a key role in determining the cost and reliability of an RF system. Figure 15 shows a thermal image of the 200 W device of Figure 7(a) under the condition of 80 W of dissipated power. The results show a maximum channel temperature of approximately 98 ºC. This corresponds to a thermal resistance of approximately 1ºC/Watt. While this is certainly sufficient for backed off operation in a Doherty amplifier or pulsed RF application, lower thermal resistance is likely needed for CW applications.

Data from published GaN device reports illustrate these thermal limitations. Figure 16 shows power density versus drain bias for GaN devices reported in the literature. The plot shows reports of up to 40 W/mm (16 W) on a 0.4 mm device at 120V [4]. On the other hand, LDMOS devices generally operate at 48 V and below at a lower current density than GaN devices. Therefore their power density is generally in the vicinity of 1-2 W/mm. However, with improved substrate and packaging, it may be possible to further increase the power density for GaN devices.

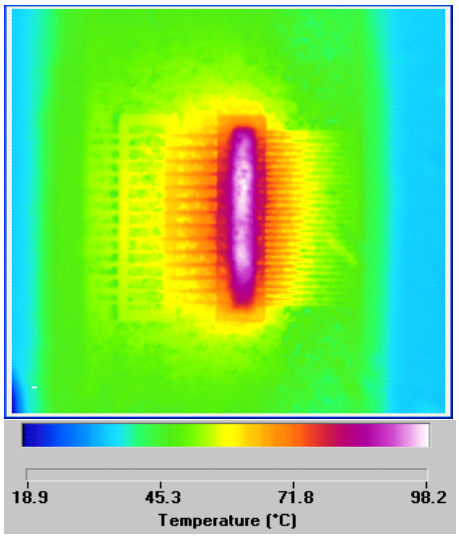

Figure 15: Thermal image of 200 W device of Figure 7(a) showing a a thermal resistance of approximately 1 ºC/Watt.

Despite the possibility of operating at much higher than 10W/mm, devices that operate at the hundred watt level and higher tend to operate at much less than 10 W/mm to keep the channel temperature sufficiently low. Figure 17 shows that power densities for GaN devices in the 200W range are limited to less than 10 W/mm in pulsed operation and about 4-5 W/mm for CW operation. On the other hand, LDMOS devices show well behaved power scaling with increasing power density: As the power density increases, the total power increases. This observation shows a significant thermal limitation for GaN on SiC technology for very high power levels. To address this, improved thermal management is needed.

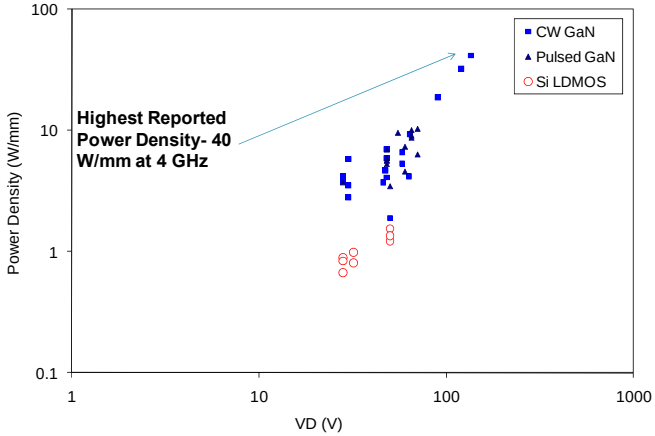

Figure 16: Power density vs. drain voltage for GaN and Si LDMOS.

Thermal simulations, summarized in Figure 18, indicate that approximately 40-50% of the thermal resistance is due to the GaN and SiC substrate while 50-60% of the thermal resistance is due to the package. The GaN on SiC substrate imposes a significant thermal resistance because the GaN nucleation layer between the GaN and SiC is amorphous and amounts to a thin but potent thermal insulator. For this reason, some companies have developed GaN on diamond substrate technologies [5]. These solutions promise to dramatically reduce the R_{th} component associated with the substrate. However, even with a lower R_{th} substrate, improved die attach and package material is needed to realize the benefit. To this end, we are developing advanced packaging and die attach materials to improve the overall R_{th} of a large packaged device.

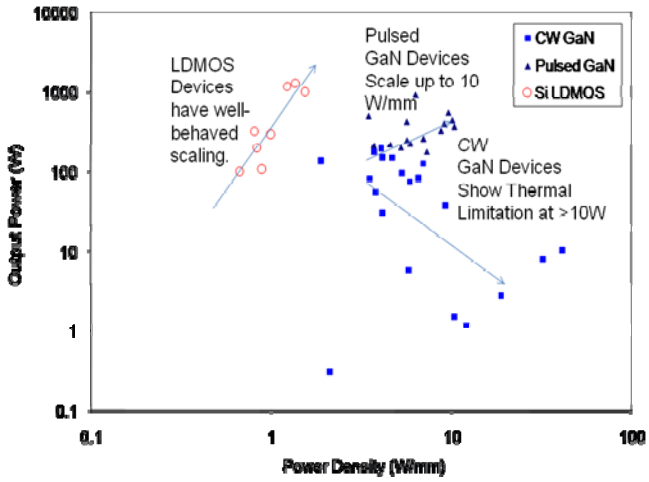

Figure 17: Output power vs. Frequency for GaN and Si LDMOS. GaN Provides High Power Beyond 2.5 GHz.

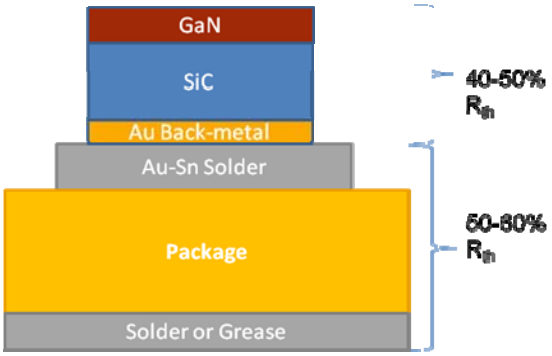

Figure 18: Schematic of materials stack for a packaged GaN HFET transistor.

VII. Cost v. Performance and the Choice of Substrate

The prior sections have demonstrated the performance and size advantages of GaN devices. Besides the technology maturity and yield issues that continue to be addressed, higher cost for GaN has kept it from enjoying widespread adoption. The somewhat higher cost of GaN will only be accepted if there are no viable alternatives. Since LDMOS has been surprisingly competitive even at 2.5 GHz, LDMOS has been chosen for many class AB and Doherty PA applications. However, for high efficiency architectures such as switch-mode PA's and for high frequency amplifiers beyond 3.5 GHz, there are no viable alternatives to GaN. As these

architectures are adopted, GaN will be used in volume and its cost will continue to drop.

The substrate has the greatest influence on the cost of GaN technology. Other costs such as materials growth and processing are similar to those of GaAs in sufficient volume. As seen in Table 3, SiC has high thermal conductivity along with low losses at high frequency; high cost is its only downside. SiC substrates allow the step function improvements for GaN with enough maturity and a low enough price to be viable. However, because GaN on SiC technology has really just started to become mainstream within the last 5 years and volumes have just started to increase in the last 2-3 years, the substrate cost has been kept somewhat high. For now, this makes GaN on SiC die significantly more expensive than Si LDMOS. In time, it is expected that the cost of the SiC substrate will approach that of GaAs and that the cost difference will be less significant.

Alternative substrates either lack performance or are too expensive. High resistivity silicon is a lower cost alternative with moderate thermal conductivity and high frequency capability; the low cost motivates low frequency power switch vendors to use Si as a substrate. Unfortunately, Si loses its high resistivity at 150º C temperature giving it less appeal for high efficiency RF applications. GaN substrates, while available, are very expensive because they must be grown at extremely high pressure or by CVD techniques. In recent years, much progress has been made in bonding GaN to CVD diamond that promises 3X higher thermal conductivity than SiC [5]. Since it is less mature, more expensive, and un-proven, it has not been adopted.

Table 3: Comparison of possible substrates for GaN devices.

Material	Thermal Cond.	High Frequency Perf.	Wafer Diameter	Cost	Volume Driver
SiC	High	Good	75-150 mm	High	Opto-Electronics Power Devices
CVD Diamond	Very High	Good	50-100 mm	High	Thermal Heat Spreaders
Si	Medium	Poor	>100 mm	Low	MOSFET
GaN	Medium	Good	50-75 mm	Very High	Opto-Electronics

VIII. Conclusion and Prospects for Future Applications

We have discussed the technology, device performance, Doherty power amplifier performance, and thermal management of GaN devices and have shown that GaN complements LDMOS technology for high frequency, beyond 2.5 GHz applications where LDMOS impedances become difficult to manage. In spite of its truly impressive performance to date, GaN still has much untapped potential.

Improved thermal management at the substrate and package level will allow the technology to operate at higher performance and duty cycles. Also, while GaN has shown high performance operation at 2.5 GHz and below, its cost may not justify using it to replace LDMOS for narrow-band amplifiers where the size of the amplifier is not a concern.

We believe that GaN's biggest impact will be seen in PA applications such as switch-mode PA's and very wideband PA's. Here, LDMOS does not provide a viable alternative to GaN because of the high power needed at 2nd, 3rd and higher harmonic frequencies for these applications. Thus, GaN technology has brought about a renaissance of high efficiency amplifier architectures such as class E [6], class F [7], class S [8], that until now, have been confined to audio and VHF/UHF frequencies because of lack of power at higher harmonics using LDMOS.

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