The Quest For A Rugged Transistor

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Traditional RF applications required power transistors that could withstand high mismatch conditions, but the ability of the latest generation of devices to handle even more severe mismatches has enabled new and emerging high-power RF applications, as well as dramatically improving reliability and simplifying more mature applications.
High-power transistors undergo a great deal of abuse, even when designed into well-conceived circuits. In a communications system, for example, a damaged antenna feeder can result in severe impedance mismatch conditions presented to the load of a device. At high-power levels, a mismatch can result in currents and voltages exceeding device ratings. Higher transistor operating temperatures and stresses due to mismatch can lead to problems with reliability and shorten device operating lifetimes. While there is no simple way to avoid load mismatch and the associated stress and generation of heat, the negative effects can be minimized by specifying transistors that are designed to be rugged and have superior thermal properties. One such transistor is the MRFE6VP61K25H, the highest power device in a complete line of enhanced ruggedness silicon laterally diffused metal-oxide-semiconductor (LDMOS) transistors from Freescale (www.freescale.com).

All of the devices in Freescale’s enhanced ruggedness portfolio are produced with a EVHV6 50V semiconductor process that features a unique device configuration. These transistors are designed to be exceptionally rugged and include enhanced electrostatic-discharge (ESD) protection circuitry, arming them with improved tolerance to high load mismatches and extreme operating conditions. This makes these transistors using the EVHV6 process ideally suited for nontraditional solid-state applications where transistors are subject to less-than-ideal operating conditions. The portfolio includes devices from 300W to 1.25 kW output power over frequencies ranging from 1.8 to 860 MHz.

The latest variants of high-power RF/microwave transistors (including those based on LDMOS, gallium nitride (GaN), and even silicon carbide (SiC) semiconductor processes) are often associated with applications in cellular base station and radio/television broadcast transmitters. However, the emergence of higher-voltage (50V) LDMOS devices, such as the MRFE6VP61K25H device from Freescale, are capable of output power levels of 1.25 kW CW per device over frequencies ranging from 1.8 to 600 MHz. These high-power devices expand the possibilities and enable these devices to be used in nontraditional applications, including laser-exciter circuits, plasma generators and even in medical applications, such as magnetic resonance imaging (MRI) systems.

Such applications are routinely subject to severe load mismatch conditions, often running a high-power transistor amplifier into the equivalent of a short or open circuit. Earlier generation power transistors not designed for these high load mismatch conditions would suffer degraded performance, decreased reliability and operating lifetimes and, in extreme cases, device failure.

An impedance mismatch between a source and a load can occur from any number of causes, including transmission-line faults, bad transmitter switches and in the normal starting condition of gas lasers and plasma generators. Under ideal impedance matching conditions, the maximum amount of power from a source, such as a power transistor or an amplifier, is transferred to the load, such as an antenna. The degree of mismatch between a source and a load is usually quantified in terms of reflection coefficient or voltage standing wave ratio (VSWR). For example, under ideal conditions, all power is transferred from the source to the load and the circuit is said to have a VSWR of 1:1 and a reflection coefficient of 0. In this case, all of the power is transferred and no power is reflected. But when a transistor is attempting to drive power into a short circuit or an open circuit, it will not transfer any energy to a load and has the potential to generate infinite standing waves—a condition said to be the equivalent of a VSWR of ∞:1 or a reflection coefficient of 1. Purely capacitive or inductive loads can also bring about these infinite VSWR conditions. Such conditions can be duplicated when an antenna is blown off a mount during a storm, for example.
Between these extremes lie more typical “real-world” values of VSWR, which are found in actual operating environments. For example, at a slight mismatch between source and load (represented by a load VSWR of 1.5:1), 4 percent of the power is reflected and 96 percent of the power is transmitted. The resulting reflection coefficient is 0.20. Such conditions are often also evaluated by means of the loss due to reflected energy, or return loss, which is 14 dB in this case. For a slightly higher mismatch between the source and load, such as a VSWR of 3:1, 25 percent of the forward power is reflected back to the source and only 75 percent of the power is transmitted from the transistor or power amplifier. This condition represents a reflection coefficient of 0.50 and a return loss of 6 dB. As the mismatch conditions grow more severe, the amount of transmitted power decreases and the amount of reflected power increases, resulting in increasing values for the reflection coefficient and decreasing values of return loss.

When the impedances of the source and load are not fully matched, some of the generated power will be reflected back to the source. Because the forward and reverse waves are out of phase with each other, they can combine both destructively and constructively; resulting in decreases and increases, respectively, of voltage and current. Depending on how the forward and reflected waves interact, a sufficiently poor match can expose a device to conditions that exceed its operating limits; whether the transistor is operated under continuous-wave (CW) or pulsed conditions. The reflected energy can also cause unwanted heating effects in a semiconductor device, leading to degraded performance or even premature device failure.

In terms of ruggedness, the requirements and expectations of transistor specifiers have changed dramatically over the past decade. Early high-power LDMOS, vertical MOS (VMOS), and even GaN high electron mobility transistor (HEMT) devices were typically rated as being rugged when capable of operating into a load equivalent to a VSWR as high as 10:1 and often only 5:1. Requirements for more rugged devices driven by newer applications such as laser exciters, have pushed expectations for ruggedness to load VSWRs equivalent to a 60:1 VSWR, and higher. Some commercial power transistor manufacturers have made claims of devices that can operate into load mismatches as severe as a VSWR of 125:1—essentially claiming the devices can survive operation into near-perfect short circuits or open circuits, although such operating conditions are difficult to duplicate in test environments.

In comparing different power transistors for ruggedness, it is important to consider the operating conditions under which the load VSWR was determined. As an example, the data sheet values for the MRFE6VP61K25H LDMOS transistor from Freescale state that the rugged device can withstand operation into load mismatches as severe as VSWRs greater than 65:1. These are extremely severe mismatch conditions, but the data sheet supports these claims by providing a full set of operating conditions under which the RF performance parameters transistor are tested: 50 VDC bias, test frequency of 230 MHz, 1.25 kW peak pulsed output power, with 100 µsec pulses at a 20 percent duty cycle. The ability to handle high VSWR is tested under more severe conditions: 3 dB overdrive, 20 percent overvoltage over all phase angles. Any comparison of this transistor with another so-called “rugged” device can only be fair when the test conditions are equivalent, including the VSWR at all phase angles.

These severe tests assure that a device can handle even the most difficult operating conditions found in real applications, including the severe conditions of laser exciters and plasma generators.

While it may not be possible to “normalize” the operating conditions for all power transistors under consideration for a given application, these baseline conditions allow a designer to understand that the device can withstand a sizable load mismatch under full-power conditions while running at a full-rated bias supply. Specifiers should be wary of power transistors rated for extremely high load mismatch values that have been tested at less than full output power levels or at decreased bias levels.
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For example, high-power LDMOS transistors are typically tested for load mismatch tolerance at their 1 dB compressed output power levels, although devices such as the MRFE6VP61K25H can also operate at load VSWRs as high as a 65:1 VSWR when running beyond 3 dB compressed output power. Typical high-power GaN HEMTs are characterized for severe mismatch operation at their 3 dB compressed output power levels. Although this difference between 1 dB compression and 3 dB compression output levels may seem trivial, there is a significant difference in the stresses seen by the output device when “overdriven.” This overdriven condition of operation is common in amplifiers used in a system with power-control loops or analog or digital predistortion circuits.

Running the VSWR tests into all phase angles ensures that a device is evaluated with high current flows during lower impedance conditions and with high voltage swings during higher impedance conditions. The higher current conditions tend to induce thermal effects in a device under test, while the higher voltage conditions can push a device closer to its breakdown voltage. In some cases, high-power device failure may not even require that the transistor’s breakdown voltage be exceeded. Rapid changes in voltage can lead to device damage due to bipolar snapback. When VSWR testing has been performed at all phase angles for a rated VSWR, a specifier can be assured that the device will survive severe load mismatches under best and worst-case conditions, regardless of the phases of the source and load impedances.

Measuring Mismatch

Testing solid-state devices for mismatch tolerance becomes more challenging as the devices are made more rugged. Such testing requires presenting different, severe, but well-characterized mismatch conditions to a transistor with a calibrated, repeatable test setup. Under low-power conditions, and with load mismatches that are relatively moderate (equivalent to a VSWR of about 10:1), a passive load-pull tuner can emulate the required impedance mismatch. But as devices are being made more rugged, higher-load VSWRs are needed. Load-pull tuners, which are designed for small-signal applications, are inadequate to the task of presenting large impedance mismatches to a high-power transistor.

For that reason, special circuits or “mismatch boxes,” based on a number of custom-designed circuits, are used to present different impedance matches at specific angles to a high-power transistor under test. These circuits and mismatch boxes are built to withstand the high output power levels delivered by a device such as the MRFE6VP61K25H; whereas alternative means of testing, such as a load-pull tuner, would suffer damage from the high-power levels.

Of course, a mismatch box can only achieve maximum mismatches over a limited range of phase angles. The maximum VSWR for a given mismatch box is typically at only one phase or, at most, a small number of phase angles for a given test frequency. Since it is extremely difficult to maintain that maximum VSWR across all phase angles, it is necessary to specify minimum mismatch for a given test setup with the maximum being less controlled.

In terms of device ruggedness, an important corollary of tolerating high load mismatches is the capability of also being able to effectively dissipate heat. In any transistor, if the temperature within the device exceeds its thermal rating or rated junction temperature, device failure can result. In addition to high mismatch tolerance, devices fabricated with Freescale’s EVHV6 50V LDMOS process, such as the MRFE6VP61K25H, are designed for excellent thermal characteristics.
To better understand the thermal characteristics of these devices, they are evaluated for both pulsed and CW performance. For example, when testing a MRFE6VP61K25H high-power LDMOS transistor under different pulsed conditions (Fig. 1), shorter pulse widths tend to yield lower measured values of thermal impedance. For 100 μsec pulses at a duty cycle of 20 percent, the junction-to-case thermal impedance $Z_{\theta_{jc}}$ was measured at 0.03°C/W. Under the CW condition for the same device, the junction-to-case thermal resistance was measured at 0.15°C/W. The dissipated power, $P_D$, is the instantaneous dissipated power, and not the average dissipated power. The dissipated power, $P_D$, multiplied by the thermal impedance from Figure 1, gives the temperature rise between the junction and case temperature. Once the case temperature is known, the junction temperature can be derived.

When the same device was evaluated for mean time to failure (MTTF), which is highly dependent on a number of different factors (including temperature, drain efficiency and output power), it was found to be about 4.5 million hours of operation for a device junction temperature of 150°C (Fig. 2). This assumes device CW output power of 1.25 kW, drain voltage of 50 VDC, drain efficiency of better than 74 percent and device flange temperature of about +85°C.

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**Figure 1.**
MRFE6VP61K25H Transient Thermal Impedance
This graph shows the thermal junction characteristics of the MRFE6VP61K25H LDMOS transistor under different pulsed conditions.

**Figure 2.**
MTTF Versus Junction Temperature for MRFE6VP61K25H
This graph shows the MRFE6VP61K25H LDMOS transistor to have a projected mean time to failure (MTTF) of about 4.5 million hours, or 513 years, with a device junction temperature of 150°C.
Freescale’s high-power LDMOS transistors, such as the MRFE6VP61K25H, are housed in air-cavity ceramic packages capable of dissipating large amounts of heat efficiently. Freescale is also working on a lower-cost over-molded plastic (OMP) package version of the 300W, 1.8 to 600 MHz push-pull version of the LDMOS transistor. This package incorporates high thermal conductivity metallic flanges for effective heat flow away from the device junction. With more than 80 million devices already supplied in these OMP packages, Freescale has established a proven track record for reliability of high-power transistors in these packages. The thermally-optimized packages exhibit junction-to-case thermal resistance with 0.24°C/W for a typical single-ended part rated at 300W output power.

Silicon LDMOS transistors represent cost-effective solutions for amplifier designers in need of extremely high output power levels for both CW and pulsed applications through 2 GHz and higher. They are a fraction of the cost of devices fabricated with competing technologies, such as GaN HEMTs. They are extremely rugged and capable of high efficiency with proven reliability. In short, silicon LDMOS devices fabricated with Freescale’s EVHV6 50V process offer long operating lifetimes that can withstand the abuse of emerging high-power RF applications, including plasma generators and laser exciters.