The W3J128M64G-XSBX, W3J256M32G-XSBX and W3J2256M16G-XSBX are the 2nd devices of WEDC's high density/high performance family of DDR3 SDRAM's designed to support high performance processors, and chipsets including the Intel® 45 Express chipset.

**Product Features**
- DDR3 Data Rate = 800, 1066 Mb/s
- VDD = VDDQ = 1.5V± 0.075V
- Differential bidirectional data strobe byte
- 8-bit prefetch architecture
- Eight internal banks for concurrent operation (Per DDR3 SDRAM Die)
- Auto Refresh and Self Refresh Modes
- On Die Termination (ODT), nominal and dynamic for data, strobe and mask
- Output driver calibration
- Programmable CAS latency: 5, 6, 7, 8, 9 or 10
- Posted CAS additive latency: 0, CL1, CL2
- CAS# Write latency = 5, 6, 7 or 8 based on tCK
- Fixed burst length of 8 (BL8) and burst chop of 4 (BC4) via the mode register
- tCK range: 400 - 553MHz
- Write leveling
- Configured as 1-Rank x 64-bit data (W3J128M64G), or 1-Rank x 32-bit data (W3J256M32G), or 2-Rank x 16-bit data (W3J2256M16G)
- 72-bit data configuration under consideration. Contact factory for availability

**Package**
- TBD x TBDmm, 208 Plastic Ball Grid Array (PBGA), TBDmm²
- 3.05mm package body thickness max
- 1.00mm pitch, with larger balls for better second level reliability

**Benefits**
- TBD% space saving
- 46% I/O reduction
- Reduced part count
- 1.0mm pitch allows escape routing between balls
- Full upgrade compatibility with WEDC 4G DDR3 MCPs
- Designed for DDR3 fly-by routing and end termination
- Suitable for hi-reliability applications
- Commercial, industrial and military temperature ranges
- Typically lower power at same data rate when compared to DDR2

* This product is under development, is not qualified or characterized and is subject to change or cancellation without notice.
Density Comparison

<table>
<thead>
<tr>
<th>CSP Approach (mm)</th>
<th>W3J128M64G-XSBX</th>
</tr>
</thead>
<tbody>
<tr>
<td>9.0 x 15.5 mm²</td>
<td>TBD mm²</td>
</tr>
<tr>
<td>TBD%</td>
<td>TBD%</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Area</th>
<th>I/O Count</th>
</tr>
</thead>
<tbody>
<tr>
<td>4 x 139.5 mm²</td>
<td>4 x 96 balls = 384 balls</td>
</tr>
<tr>
<td>558 mm²</td>
<td>208 Balls</td>
</tr>
<tr>
<td>TBD%</td>
<td>46%</td>
</tr>
</tbody>
</table>

DDR3 MCP 1-Rank x 32 Block Diagram

Typical Application for 1-Rank 128M x 32 MCP

PMG - Microelectronics (also DBA as White Electronic Designs Co.) is a wholly owned subsidiary of Microsemi Corp.

3601 E. University Drive  Phoenix, AZ 85034  Tel: 602.437.1520  Fax: 602.437.9120

info@wedc.com  1GByte 128M x64 DDR3 SDRAM Flyer  •  09/10 Rev. 1  •  MIF2081
© 2010 Microsemi Corporation. All rights reserved  www.whiteedc.com  www.microsemi.com
DDR3 8G MCP 2-Rank x16 Block Diagram

Typical Application for 2-Rank 256M x16 MCP