GaN Essentials™

AN-010: GaN for LDMOS Users

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2. Abstract

This application note will compare LDMOS versus GaN for RF power amplifier stages. Basic concepts/approximations used for LDMOS will be shown to hold true for GaN.

A comparison of equivalent output power devices will be done. This comparison will show some of the similarities of GaN and LDMOS. Differences will also be shown. Key difference to be illustrated will be the saturation characteristics of GaN.

Basic characteristics such as ruggedness, stability and combining multiple amplifier stages will also be presented.

Additional properties of GaN that are significantly different than LDMOS will be presented. One of these areas is charge trapping effects, in which the device starts to turn off. Another characteristic of GaN that is significantly different is the behavior of gate current near saturation.

Impedance Profiles

2.1. Input Impedance

Input impedances of GaN devices can be estimated and modeled identically to LDMOS and GaAs FETs. The two common techniques are based on S-parameters and small signal models. Note that this is applicable to devices without internal input matching networks.

S_{11} can be used as a direct measurement of input impedance under small signal conditions. For Class-AB amplifiers it is common to set drain current above the quiescent value to better reflect self biasing during compression. The trade-off is that junction temperature will be artificially high, which causes a slight second order change in impedance.

The other common method is to use the standard small signal FET equivalent circuit shown in Figure 1, which consists of a series RC with package parasitics. For Nitronex's NRF1 devices at 28V, $R_{IN} \approx 20\Omega \cdot W$ and $C_{IN} \approx 1$ pF/W, where W is saturated device power in watts. Package parasitics can be used to fit simulated vs. measured results, with $L_{BondWire} \approx 0.2\text{-}0.8$nH, $C_P \approx 0.2\text{-}1.0$pF and $L_P \approx 0.1\text{-}0.3$nH.

Figure 1 shows the following comparison over the frequency range of 800MHz to 3GHz

1. Blue triangle =S11 of the NPTB00025 measured at I_D = 200mA (I_{DQ})
2. Purple Box = Conjugate of Z_{SOURCE} measured at CW Power out=20W
3. Red X = Equivalent circuit model

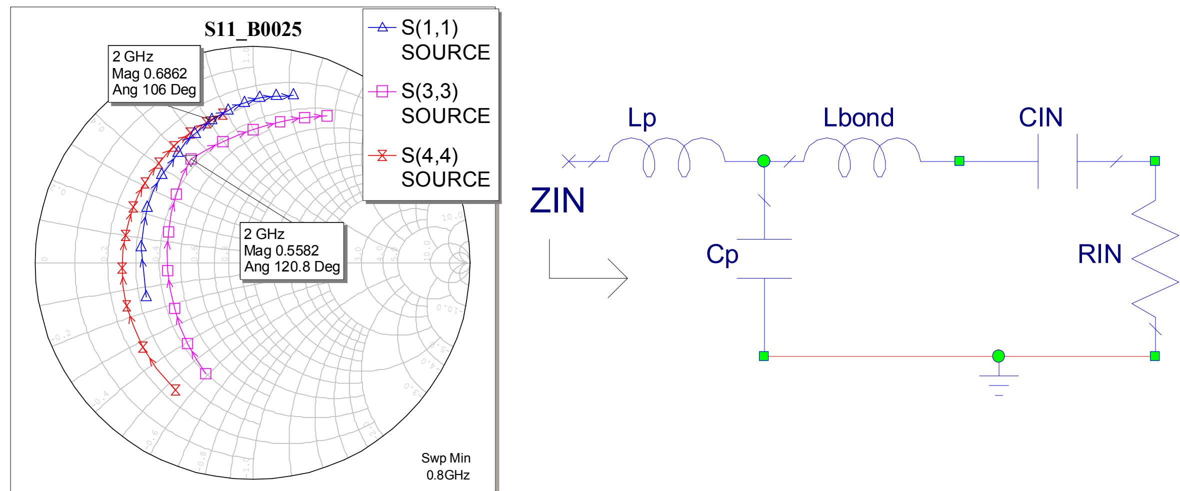

Figure 1. NPTB00025 Input Impedance Comparison Z_O=10Ω and Equivalent Circuit Model

2.2. Output Impedance

The output impedance of GaN devices can be modeled identically to other FETs such as LDMOS or GaAs. The common model for the output of a device (conjugate of optimum load impedance presented to the device leads) is shown in Figure 2 for the NPT25100.

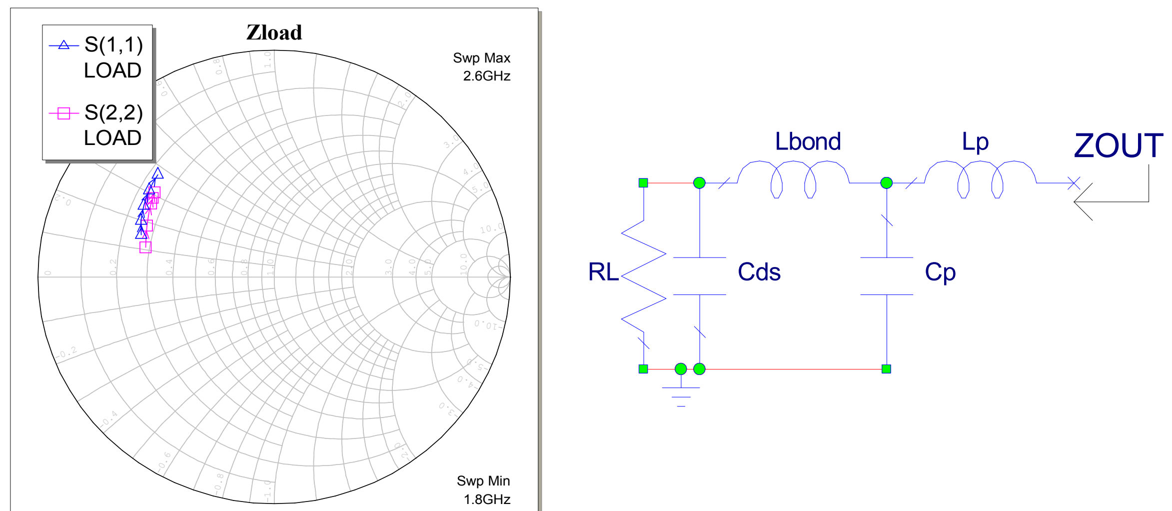

Figure 2. NPT25100 Conjugate of Z_L measured at ~100W output Compared to Equivalent Circuit Model, Z_O=10Ω Frequency range 1.8 to 2.6GHz

For current 28V NRF1 based Nitronex devices the following parameters can be used:

$C_{DS} \approx$ 0.16 to 0.20pF per W

$R_L \approx$ 500 Ω.W

$L_{bondwire} \approx$ 0.1-0.5nH

$L_P \approx$ 0.1-0.3nH

$C_P \approx$ 1.0-4.2pF

3. Stability

Small signal stability of power devices can be a difficult problem. VMOS, LDMOS, GaAs FETs, and GaN HEMTs all have large amounts of gain at low frequencies and similar challenges from a stabilization standpoint. When designing amplifiers careful attention needs to be paid to stability in both small and large signal scenarios. Smaller devices typically have higher gain than larger devices and are therefore more difficult to stabilize. The effect of a simple loading circuit upon the K stability factor for the NPT25100 is shown in figure 3 for three different loading conditions (device alone, added 10Ω resistor, added parallel RC network). This simple circuit reduces gain considerably at low frequency without affecting the device at higher frequencies.

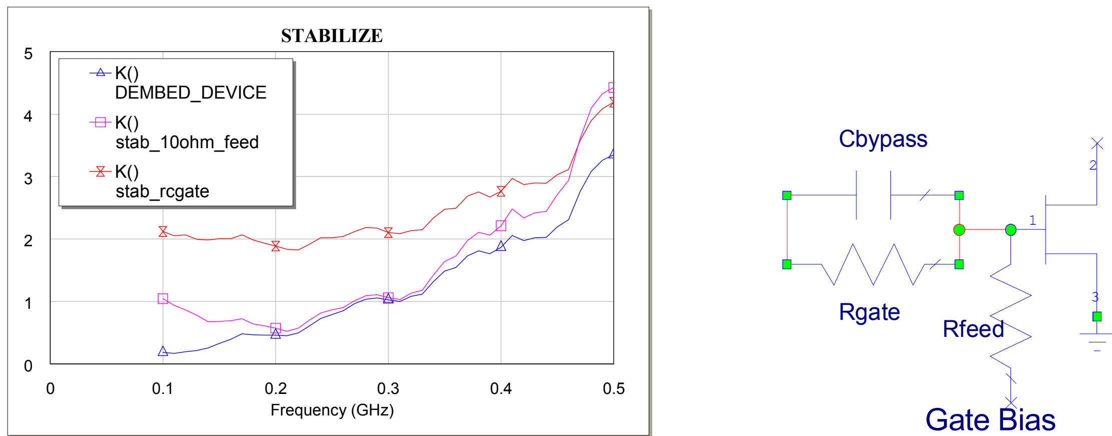

Figure 3. NPT25100 k Factor at V_{DS}=28V, I_{DQ}=300mA, Before and After Simple Loading

An in depth treatment of large signal stability analysis is beyond the scope of this paper, but a common method used for Class-AB LDMOS devices is reviewed. Small signal S-parameters are taken at various points in the bias plane and the circuit is analyzed for stability at each point. If unconditional stability is seen under these conditions, with margin for process and temperature variations, a very stable amplifier is the typical result. Figure 4 shows stability factor for the NPT25100 at various points over the bias plane from V_{DS} = 7V to 28V and I_D = 100mA to 500mA. The most difficult stability point is typically at low V_{DS} for LDMOS and GaN devices, so this point should be checked carefully. A key difference with GaN vs LDMOS is that the K-factor at 7V is approximately the same at 14 and 28V. LDMOS devices are much more potentially unstable at the lower voltages.

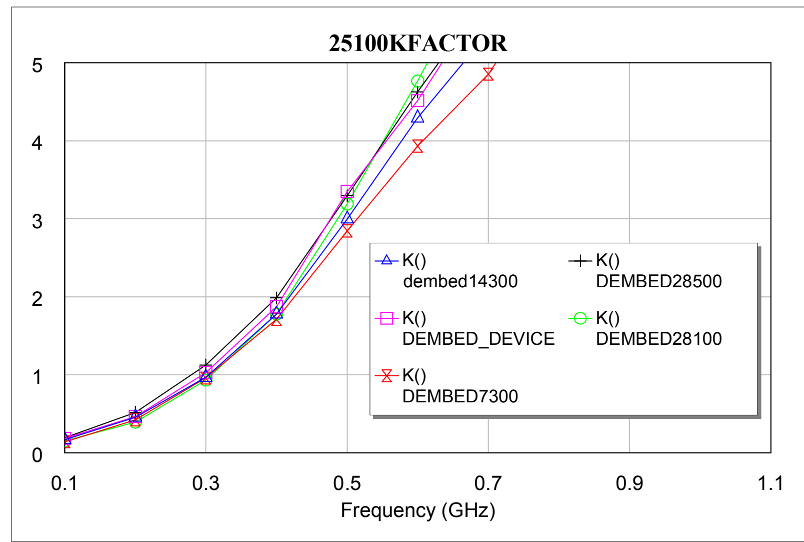

Figure 4. NPT25100 K Factor for V_{DS}=7V to 28V, I_{DQ}=100mA to 500mA, Device Alone

4. Capacitance vs. Voltage

4.1. Typical Capacitance-Voltage (CV) Characteristics

GaN HEMTs have some of the same capacitance behaviors as other FET devices. GaN's higher power density relative to the other technologies results in smaller devices and therefore smaller absolute capacitance values.

Figure 5 shows measured C_{GD} and C_{DS} vs. V_{DS} for the NPT25100. These are compared to simulated results using a TCAD model.

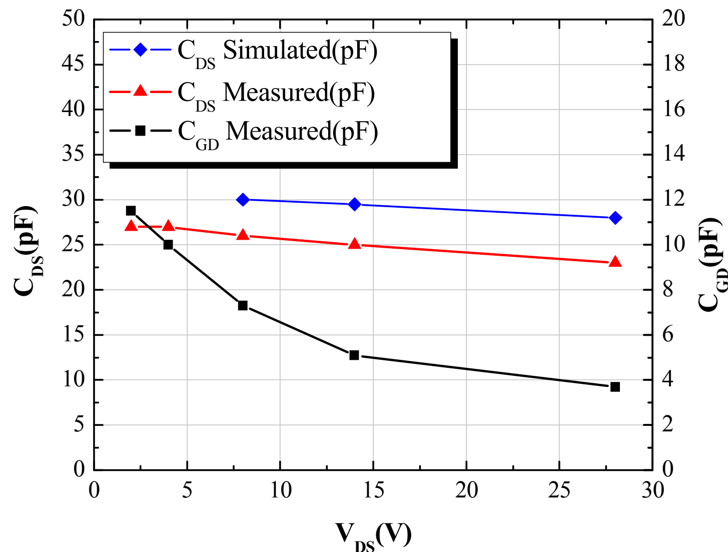

Figure 5. NPT25100 Measured and Simulated C_{GD}, C_{DS} vs. V_{DS}

A second device was measured and was typically within 1pF of the first. As the device turns on, C_{DS} will fall by ~5% at the Class-AB operating point. The change from 7V to 28V is about another 5%. The input capacitance, C_{GS}, is relatively constant at 90-100pF at I_{DQ}=600mA.

Device capacitance scales roughly linearly with FET periphery size, Table 1 lists relative scale factors for existing Nitronex devices. The capacitance of other devices can be determined by reducing the NPT25100 capacitance values by the values provided in Table 1.

Table 1. Relative Capacitance Scaling Factors for Nitronex Devices

Device	Relative Device Scale Factor
NPTB00004	18
NPTB00025	4.5
NPTB00050	2.25
NPT25100	1

4.2. Output Capacitance Comparison Between GaN and LDMOS

Output capacitance plays a significant role in determining the limitations of the bandwidth that can be achieved with a particular device. To compare various devices, the best metric is to compare capacitance per watt of output power. Table 2 shows a comparison of several commercially available devices.

Table 2. Comparison of Capacitance of Several Power Devices

Device	Rated POUT (W)	CDS (pF)	Capacitance per Watt (pF/W)
NPT25100	90	20	0.22
MRF6S9125	125	60	0.48
BLF369	500	230	0.46

For more details on broadband design using GaN see AN-013 at www.nitronex.com

5. Bias Circuits

5.1. General Bias Comments

Compared to LDMOS devices GaN has two special requirements from a biasing perspective: sequencing the gate and drain during startup and shutdown, and accommodating current flow both into and out of the gate. For detailed discussion on bias sequencing and supply circuitry see AN-009 at www.nitronex.com. Other issues such as bias network topology and general design practices are identical for LDMOS and GaN devices.

5.2. Gate Bias

Gate bias circuits for GaN devices are best implemented with a resistor feeding the gate. As a rule of thumb for Nitronex NRF1 devices at 28V, $R_G \approx 1k\Omega \cdot W$, so a 10Ω resistor would be used with a 100W device. For the NPTB0004, 100Ω is the maximum value that should be used. As with other power devices, this resistor can affect stability and should be taken into account in that analysis.

5.3. Drain Bias

Standard bias decoupling circuits used with other power devices can be used with GaN. Quarter wave lines with capacitive shorts are typical for larger devices to minimize loss. The same precautions used with LDMOS should be used with GaN to address bias line video bandwidth if required.

6. Thermal Precauations

6.1. Temperature Compensation

Nitronex GaN devices have minimal current change over temperature. The primary mechanism is electron mobility reduction with increasing temperature. The NPT25100 V_{GSQ} (V_{GS} required to hold constant I_D) over temperature characteristic is shown in Figure 6.

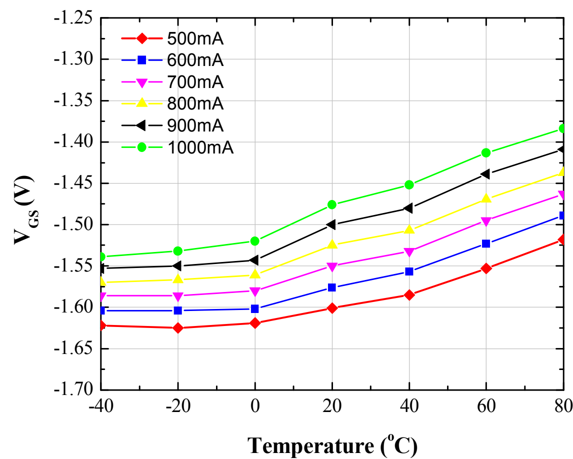

Figure 6. NPT25100 V_{GSQ} Over Temperature Characteristic

6.2. Linearity Sensitivity to Bias

Compared to Si LDMOS devices, GaN HEMT linearity is less sensitive to changes in bias point. This reduces the complexity of temperature compensation in the bias network greatly. Figure 7 shows EVM for WiMAX.

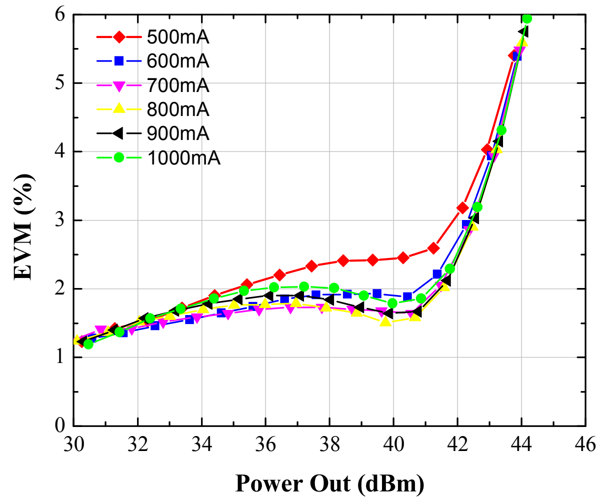

Figure 7. NPT25100 EVM vs. P_{OUT} with I_{DQ} = 500mA to 1000mA

7. Saturated Power and Compression

7.1. Typical Compression Curves

Figure 8 shows the typical compression curve of the NPT25100. GaN compression curves will become more ideal over time as future generation devices are better optimized form a thermal perspective.

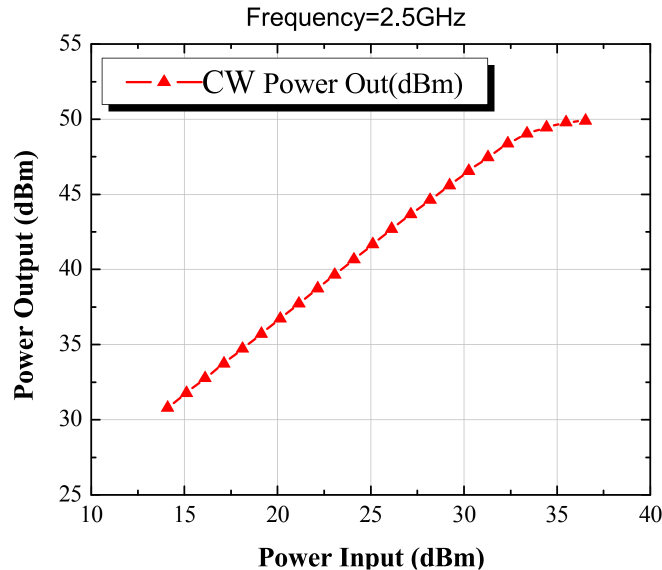

Figure 8. NPT25100 Typical Compression Curve

In pulsed or other high peak to average applications where self heating does not contribute, this compression curve can look much more ideal, with a sharper roll-off at saturation. Another point of comparison is IM3 at P_{1dB}.Table 3 shows P_{1dB}, P_{3dB}, and PEP at -30dBc IM3 for a few commercially available LDMOS and Nitronex GaN devices.

Table 3. Comparison of P_{1dB}, P_{3dB}, and PEP @ -30dBc IM3 for LDMOS and GaN Devices

Device	P1dB (W)	P3dB (W)	PEP @ -30dBc IM3 (W)
NPT25100	70	90	95
MRF5S9100	117	143	100
MRF6S9125	140	173	125

While it is difficult to make a blanket statement that holds across all devices, it is generally a more equal comparison of GaN P_{3dB} to LDMOS P_{1dB} than to compare the same compression point on both technologies.

7.2. GaN in Linearity Correction Systems

Table 3 in the previous section helps show that GaN can have good linearity past P_{1dB} compared to other devices. The inherent linearity of Nitronex 1st generation is as good as 5th or 6th generation LDMOS.

Fig. 9 shows the effect of a standard Digital Predistortion System on Nitronex GaN devices. The data is on a Doherty which consists of two NPT25100 transistors designed for WiMAX application at 2.5 to 2.7GHz. For more details, see AN-005 at www.nitronex.com.

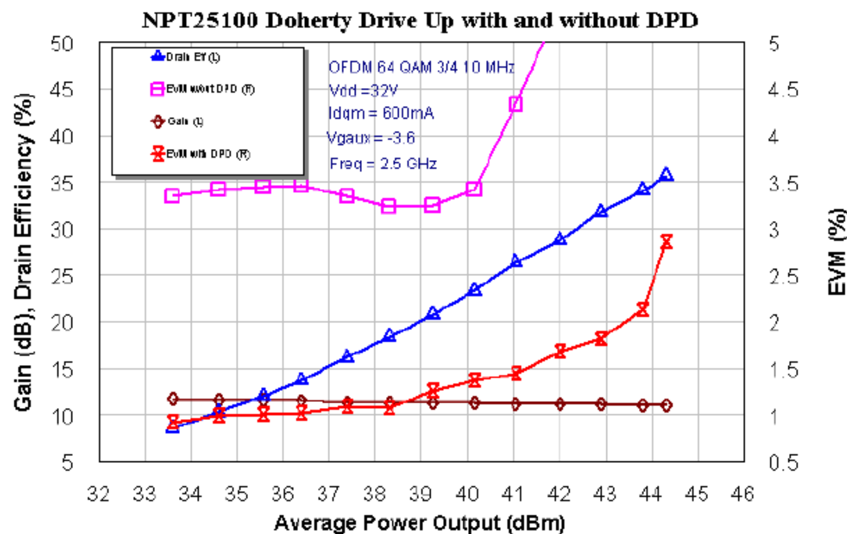

Figure 9. NPT25100 Doherty, EVM with and without DPD at 2.5 GHz

8. Robustness

8.1. Output VSWR Testing

Nitronex application note AN-004 (available at www.nitronex.com) describes stress testing of the NPTB00050 device operated at P_{3dB} and subjected to 10:1 and 20:1 output VSWR conditions. Qualification testing of Nitronex transistors included stressing devices with 10:1 VSWR mismatch, however in order to meet more stringent customer requirements characterization has been extended to a higher mismatch condition of 20:1.

Ten different NPTB00050's were subjected to a 10:1 and 20:1 VSWR condition while operating at P_{3dB}. No hard failures were observed on any of the 10 devices and no significant change in small signal gain, DE, or P_{3dB} was observed. The largest power drop from initial to post 20:1 VSWR is ~0.5dB in P_{3dB} with a median change of ~0.3dB. The test was repeated and no additional shift was seen in the devices.

The NPTB00050 device has demonstrated to be a very robust RF transistor which is capable of operating into high mismatch conditions and then continuing to deliver good RF performance.

9. Maximum RF Drive

For CW applications, GaN users may want to operate the device above P_{1dB}. An RF life test was performed on 12 NPT25100 devices. These devices were tested at 3dB compression of ~50W out and a junction temperature of 200°C. All 12 devices showed maximum degradation <0.25dB after 500 hours. Gate current was negative for all of these devices during the test.

For these devices to be used past the 1dB compression point, there are 3 criteria that need to be considered: Junction temperature, gate current, and device variation over process and temperature.

At maximum output power, dissipated power is also at a maximum. Junction temperature should always be kept below the absolute maximum limits defined in the data sheet.

Gate current must be kept below electromigration limits. GaN devices use a Schottky diode, and as RF drive is increased this diode will forward conduct, eventually causing current to flow into the gate. If this current exceeds electromigration limits, device reliability may be compromised. Table 4 shows gate current limits that should be observed.

Table 4. Maximum Gate Current for Each Nitronex Product

Device	Maximum Gate Current (mA)
NPTB00004	10
NPT25015	40
NPT35015	40
NPTB00025	40
NPTB00050	80
NPT25100	180

Device performance variation over process, external component tolerances (matching impedances), and other factors will affect the output power at which gate current turns positive. As part of a design with a GaN device being used far into compression, an estimate of the variation of circuit elements should be done to help insure that the gate current doesn't get near the max positive level. To help with this estimate, the following data shows the performance variation of the NPTB00050 into load impedances near the optimum. This can be used

for determining how much the device should be backed off from the 3dB compression for long term operation. Figure 10 shows the drive up curve into a load that gives a good tradeoff for saturated power and efficiency. Notice the rapid change in gate current as it goes positive. Gate current is negative on the order of microamps until the gain compression is ~ >2dB. From this curve you can see that the 3dB compression point is very close to the max or saturated power level.

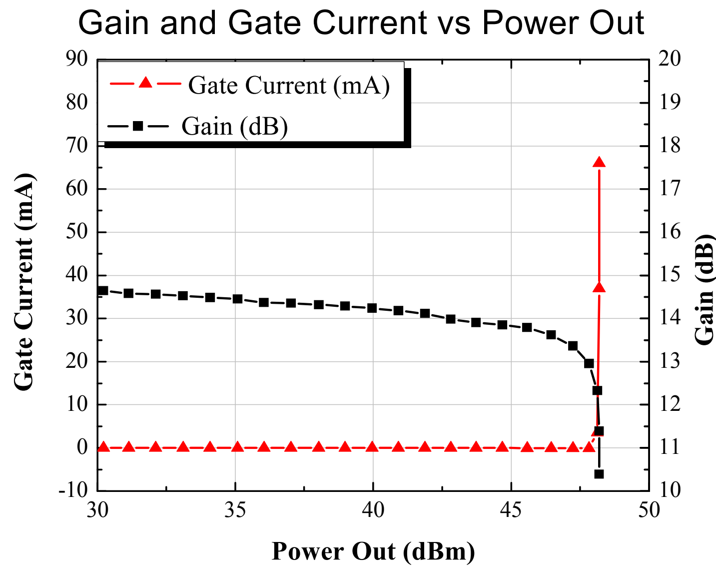

Figure 10. NPTB00050 Typical Gain Compression Curve and Gate Current (I_G)

The following test was done on this NPTB00050 device. At various loads around the chosen optimum point, the device was driven into saturation and gate current was recorded. Table 5 shows the current levels for the 3 load impedances near the optimum; Figure 11 shows the performance into these impedances along with a wider range of load impedances. At hard saturation, the gate current is still less than the max allowed of 80mA.

Table 5. NPTB00050 Gate Current Variation with Load Impedance

Load Impedance (Ω)	Compression Point 1		Compression Point 2	
	Gain Compression (dB)	I_G (mA)	Gain Compression (dB)	I_G (mA)
4.4 – j2.0	3.5	24	4.5	51
4.4 – j4.0	3.3	37	4.3	66
3.7 – j3.0	3.3	45	4.3	74

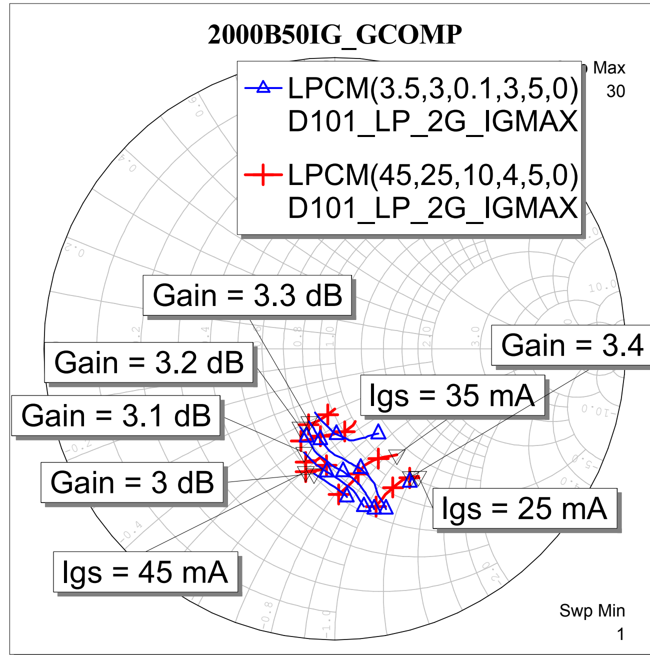

Figure 11. Graphical View of Load Impedances Used in Table 5 along with Additional Load Impedances

Blue Triangle = Gain Compression, Red + = I gate, Smith Chart Normalized to 5Ω

10. Insertion Phase Variation

10.1. Wafer and Device Variation

GaN devices amplifier stages can be combined to raise the output power of an amplifier. When combining devices/stages the key characteristic is insertion phase. Table 6 shows the data on a number of NPT25100 measured in an application circuit at 900 and 925MHz The variation is typical or better than what one would expect based on past history with LDMOS device.

Table 6. NPT25100 Insertion Phase Variation per Wafer

NPT25100 INSERTION PHASE (Degrees)			
P_{OUT}=48.5dBm,V_{DS}=28V			
Wafer #	**Dev #**	**Freq=900MHz**	**Freq=925MHz**
070713D	236	112.5	60
070713D	242	114.5	62
072126D	10	116	64
072126D	298	114	62
063322D	2	115	62.5
063322D	3	116	61

10.2. Phase Variation into Compression

When using GaN devices for CW applications and combing stages, the variation in insertion phase further into compression is important. Fig. 12 shows the change in insertion phase for a NPT25100 device as it is driven into compression.

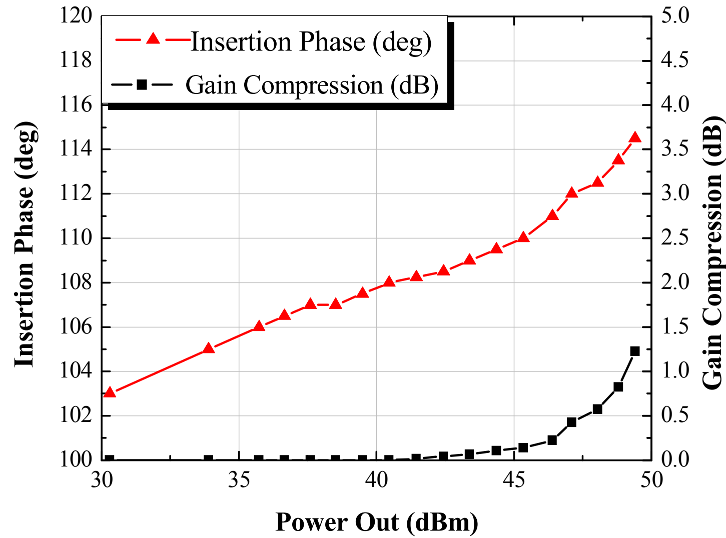

Figure 12. NPT25100 Insertion Phase and Gain Compression vs Power Out.

This data along with the results in section 10 can be used for guidelines in determining how hard a GaN device can be compressed for long term operation. This data was taken at ~900MHz, so the effect of input match variation is not included. Check back at www.nitronex.com for version 2 of this application note which will show the same data at 2.5GHz.

10.3. Phase Variation over Supply Voltage

Figure 13 shows the change in insertion phase of a NPT25100 as supply voltage is varied while input power is held constant. Additional insertion phase data was collected on the NPT25100 over a 24 to 32 V range at a constant power out of 49dBm and showed an insertion phase variation of only 2 degrees.

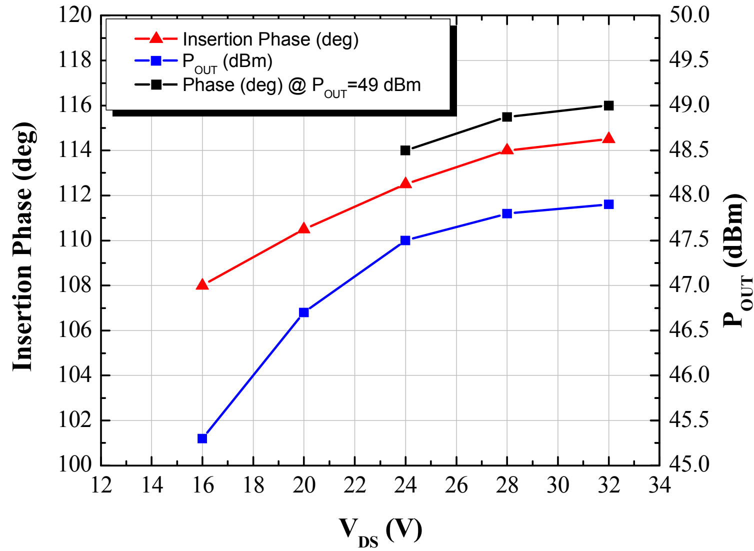

Figure 13. NPT25100 Insertion Phase and P_{OUT} vs Supply Voltage

11. Conclusions

GaN HEMT devices, while being very different from LDMOS in many ways, can generally be designed with and treated just like LDMOS FETs. GaN provides significant advantages when an application requires pushing the limits on power, efficiency, frequency or bandwidth. The data and analysis in this application note bridge the gap on many issues for designers experienced with LDMOS and now starting to work with Nitronex GaN-on-Si HEMTs. Visit www.nitronex.com for other GaN Essentials™ application notes and other information to help with your design.