GaN Essentials™

AN-011: Substrates for GaN RF Devices

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2. Abstract

The commercialization of III-nitride technology and fabrication of high quality GaN based devices has been made possible due to the advances in the deposition of III-N thin-films on Si substrates. AlGaN/GaN high electron mobility transistors (HEMTs) for high power RF applications are predominantly fabricated on either Silicon (Si) or Silicon Carbide (SiC) substrates due to the lack of native GaN substrates. The choice of the substrate is crucial and determines a wide variety of essential material properties, which in turn impact resulting device performance and reliability. Nitronex has adopted 100-mm Si as the substrate of choice; uniform substrates of high quality are affordable and plentiful due to decades of use in the microelectronics industry. The capability of Nitronex's GaN HEMT epi wafer technology is attributed to the development of novel transition layers that accommodate the stresses originating from the differences in properties of Si substrates and GaN-based materials. These transition layers result in smooth epitaxial films that are free from micropipes and other substrate imperfections which reduce performance, reliability and yield. The resulting GaN-on-Si device technology offers; (a) high power performance at high levels of reliability, (b) is ideally suited for large area RF circuits, (c) is affordable, and (d) is in high volume production today and readily available.

3. Introduction

It is well established that GaN based electronic structures, specifically AlGaN/GaN heterostructures, show clear advantages over other material systems such as GaAs, SiC, Si, & SiGe in the domain of high power and high frequency operation. The high charge density combined with the ability to operate High Electron Mobility Transistors (HEMTs) at high voltages results in devices that have ~10 times higher power density and beneficially wider bandwidths due to the resulting higher input and output impedances. GaN HEMTs also maintain their advantage of power density at high frequencies (>4GHz) when appropriate gate lengths are used and offer the best combination of power and speed of any material system. The ability to achieve device designs with wider bandwidth at higher power levels is an enabling characteristic for the preference of GaN-based technology in the advancement and adoption of high efficiency power amplifier designs by the commercial wireless infrastructure markets. The added intrinsic benefit of lower output capacitance and on resistance will allow for the ultimate realization of GaN-based drain-modulation and switch-mode architectures providing amplifiers with better than 50% system level efficiency to the wireless infrastructure marketplace. The use of GaN HEMTs also leads to substantial reduction in size, weight and power (SWAP) and result in considerable operational benefits in military communications, radar and electronic warfare applications.

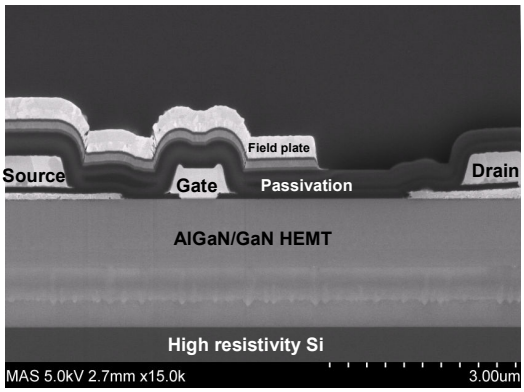

Figure 1. Cross section SEM image of 0.5µm NRF1 field plated AlGaN/GaN HEMT technology.

GaN HEMTs have been demonstrated on Si, SiC, sapphire and on native GaN substrates. However, Si and SiC are the preferred choices for RF devices. The maturity of the AlGaN/GaN heterostructures in terms of reliability, cost and manufacturability has been demonstrated through the use of commercially available high resistivity 100-mm Si

substrates. Efforts are now focused on continual evolution of the technology to improve performance and address multiple RF functions using the GaN-on-Si platform technology. Nitronex's first generation GaN-on-Si platform (NRF1) was formally qualified and released to production in October of 2006. The process was developed to meet commercial and military customers' performance needs and is qualified for operation up to 32 volts. The NRF1 process platform is inherently reliable as demonstrated with an activation energy of 2.0 eV and MTTF > 10^7 hours at T_J of 160°C[1, 2]. AlGaN/GaN on Si devices that show high performance in X-Band have also been fabricated[3]. Based on the reliability results of GaN/Si, it is apparent that GaN/Si offers superior reliability to other substrates[4] used for GaN in combination with the cost model of GaAs technology. A cross-section photograph of a fully fabricated GaN HEMT on Si substrate is shown in Figure 1. Nitronex also provides a complete qualification document for each released product which can be easily downloaded from the products section of the website.

4. GaN HEMT Epitaxy

GaN substrates (wafers) are not a viable alternative for HEMT devices and circuits due to numerous materials and economical challenges faced by the GaN substrate R&D community and the immaturity of bulk GaN crystal growth. Thus, the deposition of GaN thin films on Si and SiC is the primary approach for the fabrication of GaN RF power devices and circuits. Unlike the GaN-based LED market, the use of sapphire (Al_20_3) as a substrate for RF devices is not a viable option due to the poor thermal conductive properties of sapphire compared to that of Si and SiC.

The deposition process is broadly termed as "epitaxy" and results in a crystalline thin film on the substrate. Metal-organic chemical vapor deposition (MOCVD) is the preferred method of producing GaN-based thin films on Si or SiC for RF applications. GaN-based devices and structures have been mass-produced using MOCVD for lighting applications and the same supporting high volume epitaxial manufacturing infrastructure can be leveraged for RF applications.

Si substrates have low crystal defect density, have zero micropipes or other macro-defects, and offer a high quality surface as required for performing epitaxy. Additionally, the wafer-wafer consistency and quality are unmatched in other materials and are the result of decades of optimization of the manufacturing process of Si substrates. SEMI standard, high resistivity silicon (10^4 Ohm-cm) substrates are available through the process of zone refining of Si ingots and have very low impurity concentrations. Due to the relative lack of widespread usage and immaturity of high quality industry standard SiC substrates for RF applications, SiC standards for substrates are not established in the open literature.

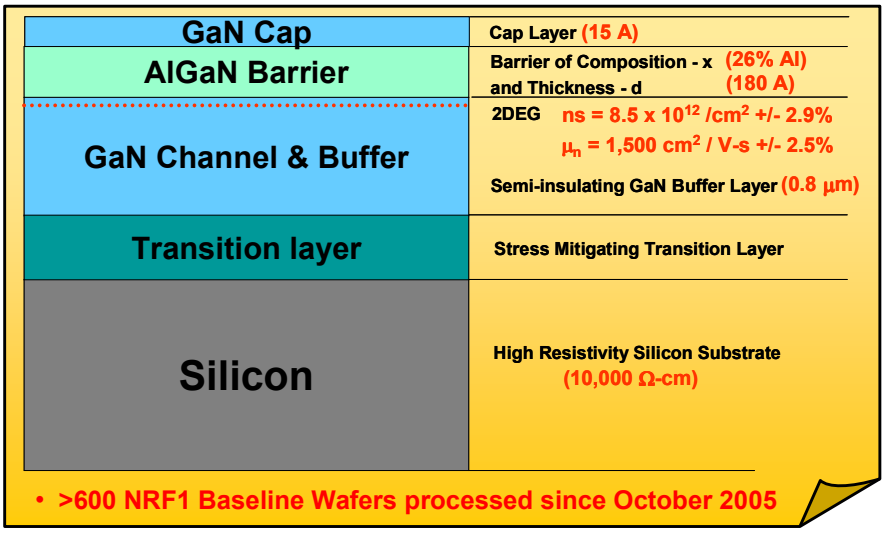

Figure 2. Schematic of NRF1 GaN HEMT material structure on Si substrate developed at Nitronex. NRF1 refers to the qualified RF process platform technology intended for applications up to 6GHz.

Growth of high quality GaN on Si (111) can be achieved by addressing the significant levels of lattice misfit (~17%) and thermal expansion coefficient (TEC) (~ 56%) mismatch. An initial layer of aluminum nitride (AlN) is deposited on the Si substrate to accommodate the strain associated in differences between crystal properties of Si and GaN. Several groups have made efforts to manage this high level of lattice and thermal mismatch[5, 6, 7, 8, 9], with varying degrees of success. At Nitronex, a novel growth process, SIGANTIC®, has been developed that results in the growth of crack-free GaN, which has been used to fabricate GaN-based devices in both microelectronic and optoelectronic areas[10, 11, 12, 13]. A schematic of the epitaxial GaN HEMT material structure is shown in Figure 2.

The absence of cracks and excellent electrical and material characteristics imply that the lattice misfit and TEC mismatch have been adequately addressed by the transition layer scheme described above. The transition layer addresses the two challenges necessary for the successful growth of GaN on Si: It manages both the lattice and thermal mismatch between the two materials. The AlN/Si interface absorbs most of the lattice mismatch while the (Al, Ga)N transition layer is successful in absorbing the stresses that arise due to the TEC mismatch. Nitronex has optimized the thickness and the nature of the composition profile of the transition layer to produce high quality films that are optimized for RF performance and reliability. The growth conditions of the transition layer have also been determined to be significant; this suggests a role played by the nature and density of defects and the resultant material properties of the transition layer.

Epitaxy of GaN HEMTs on Si substrates produces atomically smooth surfaces, which is critical for the formation of HEMTs[14]. Epitaxial films typically have several kinds of crystal defects, which can negatively impact device performance and reliability. For example, the presence of impurities in GaN films results in low RF drain efficiency. The impurities can be reduced by using high purity source materials during deposition and by optimizing the growth conditions to minimize incorporation of harmful impurities such as carbon and oxygen. Another kind of defect that has been reported to negatively impact device reliability is the presence of screw dislocations, which are a kind of thin film crystal defect that is generally present in GaN. Nitronex has developed a GaN epitaxial process that results in films that have substantially reduced pure screw dislocations density[15]. Based on transmission electron microscopy, an apparent screw dislocation density of less than ~1 x 10^7 cm^{-2} was observed. The reported high MTTF[1, 2] is attributed in part to the low density of screw dislocation defects observed in GaN/Si compared to GaN/SiC.

The GaN-on-Si platform technology is a core strength of the engineering team at Nitronex and is currently protected under US Patents 6,611,002, 6,617,060, 6,649,287, 6,956,250, 7,071,498, 7,135,720, 7,233,028, 7,247,889, 7,339, 205, 7,352,015, 7,352,016, 7,361,946 and 7,365,374.

5. Thermal Effects of GaN Substrates

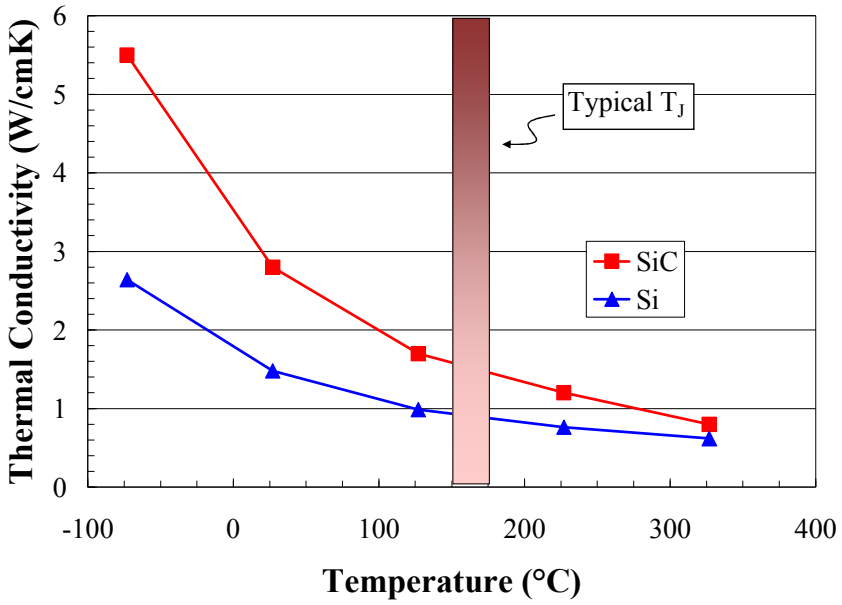

Figure 3. Thermal conductivity over temperature for Si and SiC [16].

Another aspect of choosing the appropriate substrate for GaN-based RF products is the thermal conductivity needed to design parts meeting the customers thermal design criteria. Of the two common choices, SiC has a higher thermal conductivity compared to Si. However, the extent of thermal conductivity benefit of SiC over Si is diminished by the following:

1. The thermal conductivities of Si and SiC are plotted in Figure 3. Although SiC is more thermally conducting than Si, the difference in thermal conductivity of SiC over Si diminishes as temperature increases and approaches typical operating temperatures of ~175°C.

2. The thermal resistance of the package contributes ~50% of final thermal resistance of the packaged device. Therefore, the contribution of the substrate to the final thermal conductivity is reduced.

3. The power amplifier application specific thermal resistance targets are also met through die thinning. Nitronex has achieved ~15% reduction in thermal resistance by reducing GaN HEMT on Si die thickness from 4mils to 2mils.The benefit of SiC when compared to Si diminishes as die thickness is reduced as shown in Figure 4. The temperature rise of GaN devices show reduced sensitivity to substrate thermal conductivity as die thickness is reduced as shown in Table 1. For the purpose of comparison, a 10 finger device with 200µm gate width and 25µm gate-gate pitch was simulated with a dissipated power of 3W/mm on both substrates.

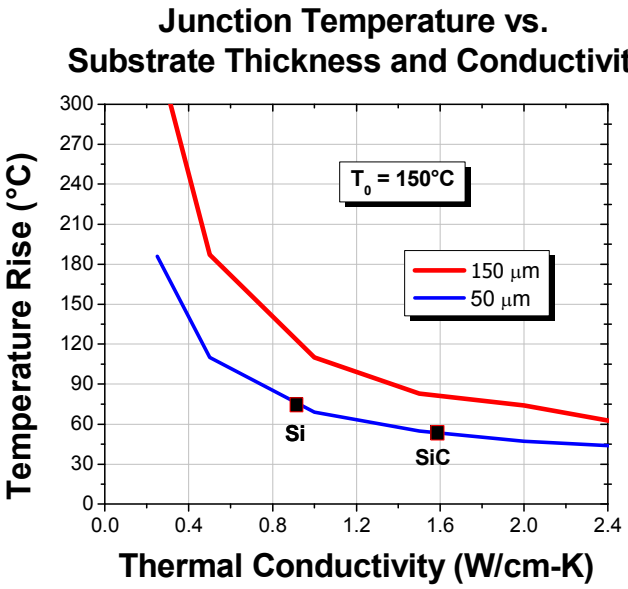

Figure 4: Temperature rise of GaN devices show reduced sensitivity to substrate thermal conductivity as die thickness is reduced. Thus, the benefit of thermal conductivity of SiC when compared to Si diminishes as die thickness is reduced.

Table 1. Temperature rise of GaN HEMTs on Si and SiC substrates for various die thickness. For the purpose of comparison, a 10 finger device with 200µm gate width and 25µm gate-gate pitch was simulated with a dissipated power of 3W/mm on both substrates.

T_0 = 150°C		Si K=0.9 W/m-K	SiC K=1.6 W/m-K
ΔT (°C)	t=150 µm	122	82
	t=50 µm	75	53

6. Cost Considerations

RF power transistors and circuits represent a significant cost of amplifiers used in both commercial and military applications. Therefore, the cost of the substrate is critical for PA applications and has an impact on final cost of the device. The cost of the RF component is dependent on substrate cost, processing costs and yield costs as discussed in greater detail below.

1. Substrate cost: The cost of a 100-mm diameter high resistivity Si substrate is ~$30-60/wafer in volumes required to satisfy all identified applications of RF power transistors. High resistivity 100-mm (4H variety) SiC substrates are not readily available in volume for purchase and are reported only in R&D quantities of a few wafers. 3-inch diameter SiC wafers are reported to be available at a cost of ~50-100 times the cost of a 100-mm Si substrate. The maximum volume of 4H SiC that is obtainable is largely unreported and is assumed to be in R&D quantities.

2. Processing costs: GaN HEMTs are processed in low volumes. Therefore, the processing cost per wafer will be likely dominated by fixed costs. Thus, the processing costs for 100-mm Si and 3-inch SiC wafer can be assumed to be the same.

3. Yield costs: Die yields affect final cost significantly because high back end costs in packaging, assembly and test cost are incurred. In case of power amplifier modules, the back end cost for a single amplifier can be hundreds of dollars. GaN MMIC PAs may occupy large areas (up to 50mm^2 per MMIC), requiring very low defect density to produce manufacturable yields. Use of Si substrates improves chips/processed wafer in three important ways. Firstly, a 100-mm wafer Si wafer is 180% the area of a 3-inch SiC wafer for an edge exclusion of 3-mm. Thus, the number of devices per wafer is increased enabling substantial cost reductions. Secondly, SiC substrates contain micropipes and other wafer imperfections, which are yield killers, while Si wafers are free from such macro-defects. Thirdly, the larger wafer area reduces edge exclusion effects during epitaxy and processing leading to increased number of chips/wafer.

It is difficult to precisely compare the cost of devices from GaN/Si with GaN/SiC. However, by making some assumptions, Nitronex has estimated the cost benefit of using GaN/Si over GaN/SiC. The key assumptions are:

1. The cost of fabrication for GaN/Si and GaN/SiC is assumed to be the same. This includes front and backside processing.

2. The yields for all GaN/Si and GaN/SiC are assumed to be identical for a given volume of wafers. However, as discussed earlier, this assumption underestimates the cost of GaN/SiC due to impact of micropipes.

This estimation is shown in Figure 5. The cost/mm^2 was calculated for 3-inch GaN/SiC, 100-mm GaN/Si and 150-mm GaN/Si. Then, all the costs are normalized to the cost of 100-mm GaN HEMTs for purposes of comparison. It can be seen that the cost of GaN/SiC is ≥3x the cost of 100-mm GaN/Si due to half the area and substantially higher substrate costs for volumes ≥ 3,000 wafers per year. For Si substrates, scaling the wafer diameter from 100-mm to 150-mm has further potential to reduce costs of GaN HEMT die.

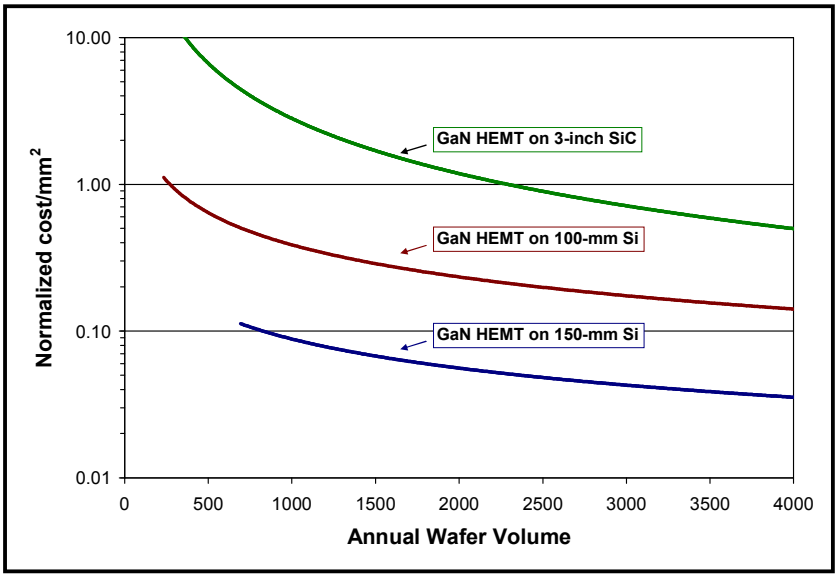

Figure 5. Estimated cost of GaN/SiC vs. GaN/Si for two different wafer sizes. The estimated costs for 150-mm GaN/Si and 3 inch GaN/SiC are normalized to the cost of 100-mm GaN/Si for comparison.

The other important aspect of substrates for GaN HEMTs is the availability. It is conservatively estimated that 2500-5000 100-mm wafer equivalents of discrete devices are required annually to satisfy the power amplifiers for the commercial wireless infrastructure market. The military applications will likely require an additional 25-50% of 100-mm wafers equivalents. The usage of large area, high power GaN MMICs instead of GaN HEMT discrete devices further increases the number of wafers required to meet the demand. Thus, it is not only important to understand the cost of the GaN HEMT wafer, but it is also essential that the required supply of substrates for GaN can be secured to satisfy the high volume applications.

What is not so obvious is the impact that the choice of substrate has upon cost, scale and the speed of product and technology development. The usage of low-cost substrates enables the development of processes with statistical process control and significantly reduces the development cost burden for the customer. For example, Nitronex has produced >15,000 GaN/Si wafers in support of the commercialization of GaN HEMTs. This scale of effort backed up by statistical process control is not feasible through the use of SiC substrates as such a large supply of 4H SiC may not exist and would be cost prohibitive. In a similar fashion, use of a Si substrate reduces cost of product development, which in turn reduces the barrier for widespread adoption of GaN for various applications.

7. Summary

GaN HEMT technology is widely recognized and accepted as the technology of choice for high power and high frequency applications that have traditionally been supported by GaAs materials. Silicon LDMOS performance drops off as the frequency of operation increases to >3GHz while GaAs suffers from low power even though it has potential to operate at high frequency. GaN on the other hand, offers higher power at frequencies up to 12GHz. At the present time and well into the future, there is no other choice but to utilize GaN for high frequency and high power applications. Relative to other GaN HEMT solutions (based on other substrates), Nitronex's GaN-on-Si offers the following advantages:

1. The use of large area (currently 100-mm) silicon substrates has dramatically improved manufacturability of GaN HEMT devices. Silicon substrates are economical, scalable, mature, of high quality, plentiful and consistent. The cost of a high resistivity silicon substrates (<$50/substrate in high volume) is a fraction of the cost of 2" high resistivity SiC substrates which are limited in quality, volume and availability)

2. Nitronex offer the longest running 100-mm GaN HEMT fabrication facility; the only one of its kind. Most of the equipment has fully depreciated and can annually run in excess of 1000 100-mm wafers with potential to scale up in volume by a factor of four. Thus, Nitronex has the ability to reduce the cost of processing the wafers significantly.

3. 100 mm GaN HEMT processing (and potential to scale to 150-mm) is inherently more cost-effective relative to SiC substrates because it allows the use of automated fabrication, assembly and testing equipment in a fashion similar to that of GaAs industry. Nitronex expect to approach the cost structure of the GaAs FET industry at similar volumes.

4. The availability of large area also allows the design and conception of large area MMICs with high yield. When it comes to MMICs, the requirement of low cost per unit area is critical because of the large semiconductor area needed for placement of passive components and interconnects.

5. The availability and maturity of back-side processes for a silicon substrate provides the opportunity for performing source via interconnects with commercial-off-the-shelf processes and equipment. The ease of thinning also negates the intrinsic thermal conductivity advantages of a SiC substrate by allowing for aggressive and advantageous thermal engineering solutions leveraging the low cost structure of silicon solutions.

6. The availability of high thermal conductivity die-attach techniques that have been developed for silicon are now directly and easily applicable to GaN-on-Si technology.

7. Nitronex was the first and, to our knowledge, the only GaN manufacturer to offer a full qualification report for the technology and for each released product. The reports detail the reliability testing performed on the devices and their results. Nitronex has demonstrated an MTTF > 10^7 hours for a junction temperature of 160°C and associated activation energy of 2.0eV. This extended operating life is partly attributable to the apparent absence of screw dislocations in GaN/Si, which is a benefit that's not currently observed or reported in GaN/SiC.

8. Nitronex is based in the United States and offers the necessary security infrastructure to the US DoD, which is critical to maintain the tactical and strategic advantages of our defense programs.

9. Nitronex is the dominant and world leader of GaN-on-Silicon solutions for RF communications. In addition, Nitronex has broad patent protection specifically targeting GaN crystal growth, GaN processing, and RF performance for RF applications

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