GaN Essentials™

NITRONEX
CORPORATION

AN-012: Thermal Considerations for GaN Technology

GaN Essentials: Thermal Considerations for GaN Technology

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2. Abstract

Thermal management of semiconductor devices is a critical issue for a design engineer. Effective control over the junction temperatures is necessary to guarantee component performance and reliability. This application note describes the thermal considerations of GaN-on-Si Technology from a component and device mounting perspective.

3. Background Theory

3.1. Thermal Equations:

The thermal resistance (θJC) in degrees centigrade per watt (°C/W) multiplied by the power dissipation sets a maximum allowable temperature difference from the case to the junction (ΔT) and provides a thermal performance target for the design. The desired junction temperature, the maximum allowed case temperature and the coupled ambient conditions determine this temperature difference. Using the device's maximum rated thermal resistance and its dissipated power, the design engineer knows the limitations of the power transistor and can make educated choices for heat sinks and other heat transfer components. The GaN transistor device's thermal resistance can be represented as:

$$\theta_{JC} = \frac{\Delta T}{P_{Diss}}$$

$$\Downarrow$$

$$\Delta T = \theta_{JC} P_{DC} (1 - PAE)$$

$$= \theta_{JC} P_{Out} \left(\frac{1}{G} + \frac{1}{DE} - 1 \right)$$

The device thermal resistance is set by the device design and is determined by:

- The semiconductor material
- Current density
- Cell layout
- Die thickness
- Die attach

Package

The device level thermal design and tradeoffs will be covered in a separate application note.

3.2. Choosing Maximum Tj

The maximum temperature of the junction (T_J) is limited by two factors:

- Performance vs. Temperature: As with other semiconductor technologies, GaN device performance falls with increasing temperature. The electron mobility drop causes a drop in current and in saturated power at a rate of ~1dB/100°C.
- MTTF of the device: A common device reliability requirement is to achieve a minimum MTTF of 10^6 operating hours which corresponds to T_J=180^{0}C. The Arrhenius curve for Nitronex's NRF1 based products is shown below and can be found in the NRF1 qualification report online at www.nitronex.com

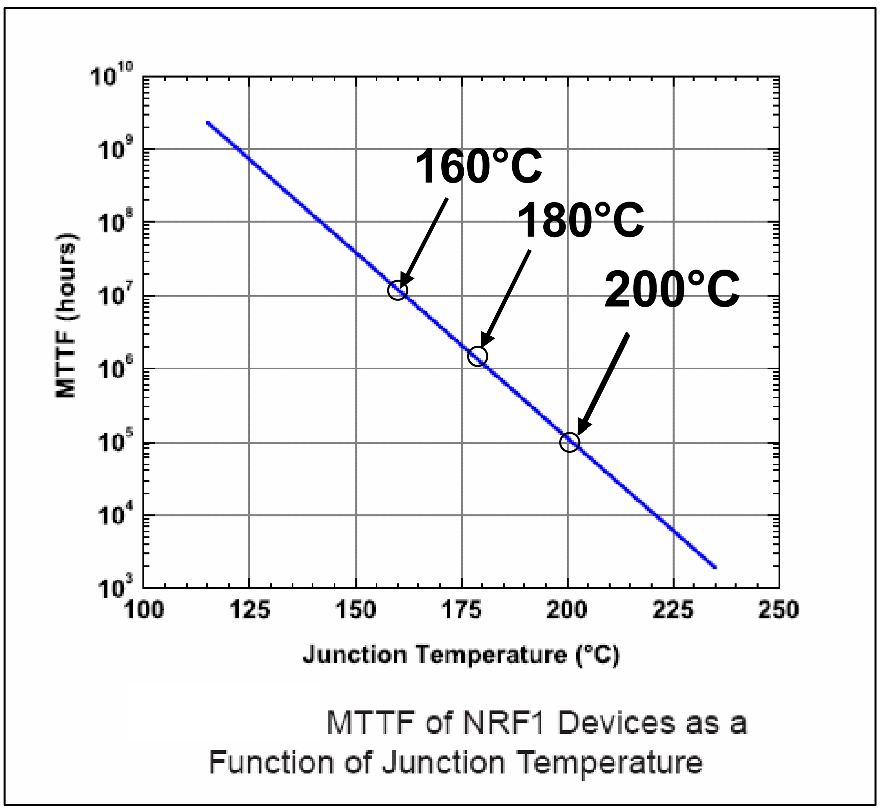

Figure 1. NRF1 MTTF vs. T_J

The device T_J is defined as:

$$T_J = T_{Baseplate_{Max}} + \Delta T \quad \Rightarrow \quad T_J = T_{Baseplate_{Max}} + \theta_{JC} \times P_{DISS}$$

$T_{Baseplate}$ is set by the customer's application: heat sinking capability, baseplate temperatures of ambient or fan-less cooling can result in temperatures up to 100 to 110^{0}C.

4. PSOP Thermal Design

4.1. Printed Circuit Board with Vias

The typical thermal problem of power amplifier (PA) designs is the difficult challenge of transferring heat from the power transistor to ambient surroundings. Figure 2 illustrates this problem for a PSOP style package surface mounted to a printed circuit board (PCB).

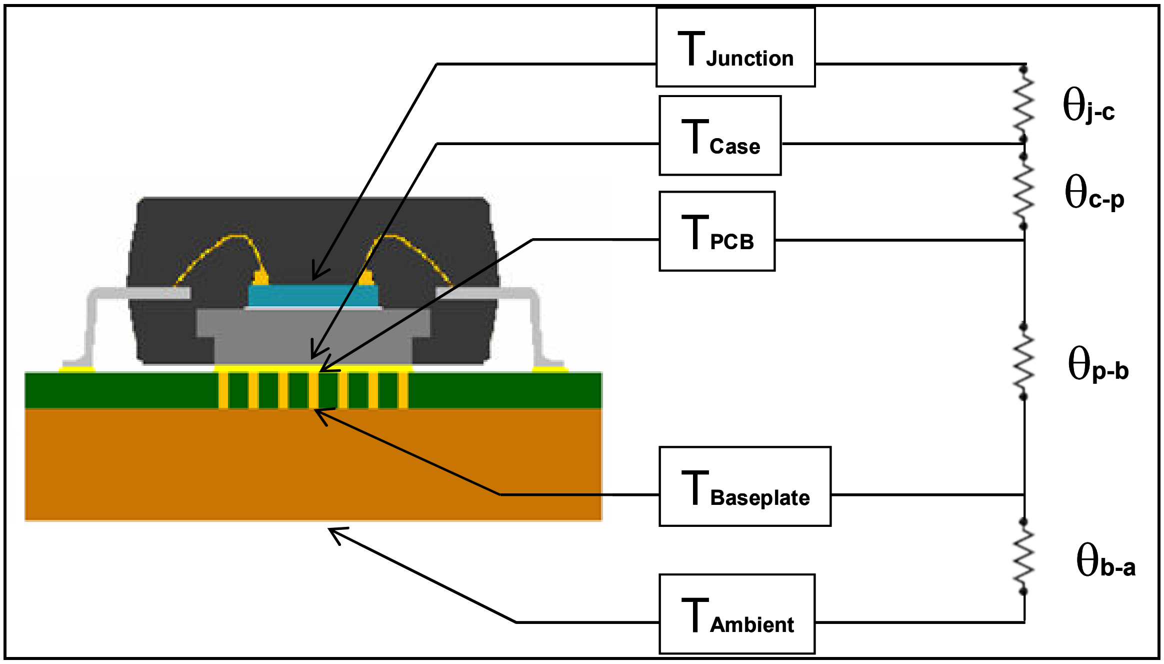

Figure 2. Thermal Stack of PSOP Package Mounted to a PCB with Vias

For a given power device and system requirement combination there are several fixed parameters that must be considered for worst-case conditions:

1. MTTF: determines maximum junction temperature
2. Worst case base plate temperature
3. $\theta_{j\text{-}c}$ as given by the device manufacturer
4. Maximum dissipated power as determined by datasheet, bench measurements, simulations and/or experience.

From these parameters, the maximum allowable thermal resistance from the power transistor case to base plate temperature can be calculated as:

$$\theta_{j-b_{Max}} = \left(\frac{T_{J_{Max}} - T_{Baseplate_{Max}}}{P_{Diss_{Max}}} \right)$$

Where,

$$P_{Diss_{Max}} = V_d I_d - P_{Out} + P_{in}$$

$$T_{J_{Max}} = 180^{\circ} C$$ (See section 3.2)

$$T_{Ambient_{Max}}$$ (Determined by system specifications)

$$\theta_{c-b_{Max}} = \theta_{j-b_{Max}} - \theta_{j-c}$$

Section 4.3 presents some thermal calculations on Nitronex's current plastic packaged product offering. Directions and guidelines for thermal management solutions (Via farm vs. Copper Insert) are given.

4.2. Printed Circuit Board with Copper Insert

It will be shown, with the PSOP2 package, for power levels greater than approximately 5-10W a standard PCB with vias will typically have too much thermal resistance to meet worst case CW saturated application design targets. Figure 3 shows a PCB with a copper insert, which greatly improves c-b, allowing up to 15-18W dissipated power.

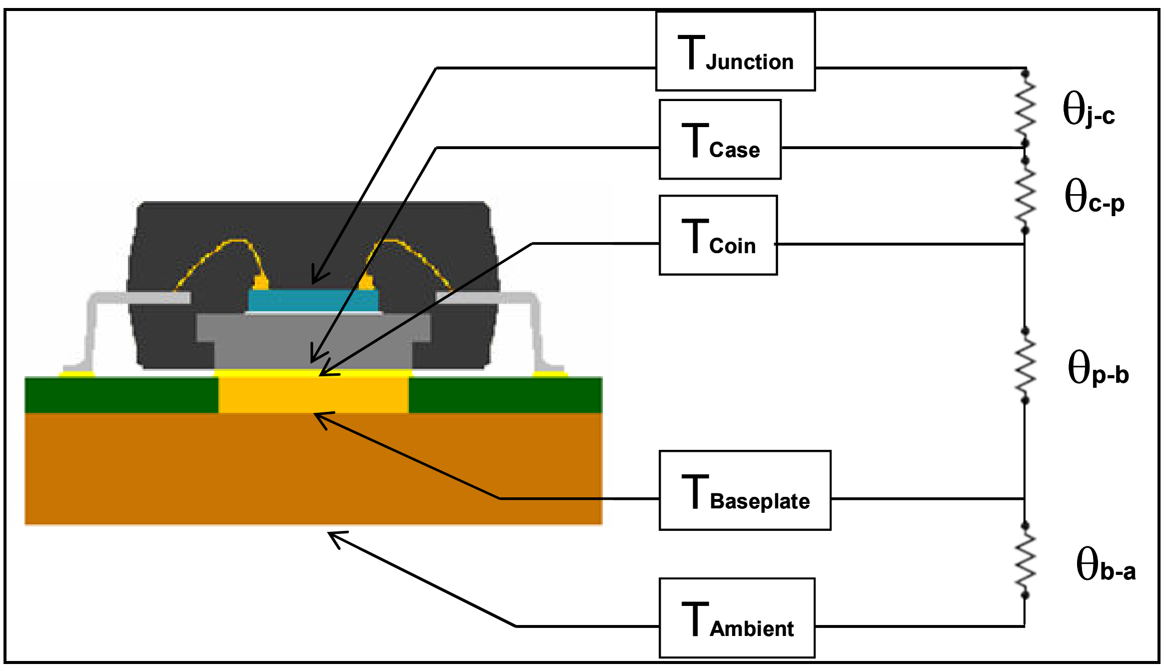

Figure 3. Thermal Stack of PSOP Package Mounted to a PCB with a Copper Insert

4.3. Nitronex Plastic Packaged Parts

This section presents some thermal calculations for Nitronex's current plastic packaged product offering for CW and WiMAX Applications.

4.3.1. CW Applications

Table 1 presents Nitronex plastic part thermal calculations for CW applications. Typical thermal resistance and CW output power, gain and drain efficiency values were taken from the latest product datasheets. Values for ΔT and T_J were calculated using equations from sections 3.1 and 3.2.

The following assumptions were made:

- The baseplate temperature is maintained at 70°C
- The performance data is taken at 2.5GHz, except for NPT35015 which is at 3.5GHz.
- Data utilized for gain, Pout and drain efficiency was taken at 25°C. Calculations are optimistic because they do not take into account effects of temperature on Pout, gain and drain efficiency.

Table 1. Nitronex Plastic Part Thermal Calculation Table for CW Applications

Device	P_{OUT} (W)	Gain (dB)	Drain Efficiency (%)	θ_{j-c} (°C/W)	P_{DISS} (W)	ΔT (°C)	Tbase (°C)	T_J (°C)
NPTB00004	5	16.3	56	26.00	4.0	105.2	70	175.2
NPT25015	23	11.5	60	6.25	17.0	106.0	70	176.0
NPT35015	16	10.0	49	6.25	18.3	114.1	70	184.1
NPT1004	40	13.5	60	4.30	28.5	122.3	70	192.3

Typically designers are asked to maintain MTTF lifetimes of 10^6 hours. Utilizing Figure 3 shows that this equates to keeping junction temperatures lower than ~180°C. Calculations in Table 1 show that there is a thermal limitation on the baseplate temperatures for these plastic packaged parts.

The designer in this case needs to utilize Cu Coins or direct heat sinking to the source of these devices using a metal pedestal. To maintain acceptable device reliability the parts should be operated in pulsed, modulated or backed off applications.

The NPT1004 is a 16mm die in a small plastic PSOP package. The PSOP package is limited in its power handling ability.

The NPT35015 is a higher frequency part. The lower efficiency is the main limitation on the part's thermal performance.

Thermal imaging results of the NPTB00004 on a via farm vs. a Cu coin are presented later in section 4.4.1.

4.3.2. WiMAX Applications

Table 2 presents Nitronex plastic part thermal calculations for WiMAX Applications. Typical thermal resistance, output power, gain and drain efficiency values were taken from the latest product datasheets. Values for ΔT and T_J were calculated using equations from sections 3.1 and 3.2.

The following assumptions were made:

- The baseplate temperature is maintained at 85°C
- The performance data is taken at 2.5GHz, except for NPT35050 which is at 3.5GHz.
- Data utilized for gain, Pout and drain efficiency was taken at 25°C. Calculations are optimistic because they do not take into account effects of temperature on P_{OUT}, gain and drain efficiency.
- EVM does not exceed 2%

Table 2. Nitronex Plastic Part Thermal Calculation Table for WiMAX Applications

Device	Pout (W)	Gain (dB)	Drain Efficiency (%)	$\theta_{j\text{-}c}$ (Ω)	Pdiss (W)	ΔT (°C)	Tbase (°C)	T_J (°C)
NPTB00004 [1]	0.8	13.5	23	25.50	2.7	69.2	85	154.2
NPT25015 [1]	1.5	14.0	24	6.25	4.8	30.1	85	115.1
NPT35015 [2]	1.7	10.9	21	6.25	6.5	40.8	85	125.8
NPT1004 [1]	5	13.0	27	4.30	13.8	59.2	85	144.2

Note 1: Single carrier OFDM waveform 64-QAM 3/4, 8 burst, continuous frame data, 10 MHz channel bandwidth. Peak/Avg = 10.3dB @ 0.01% probability on CCDF, 2% EVM.

Note 2: Single carrier OFDM waveform 64-QAM 3/4, 8 burst, 20ms frame, 15ms frame data, 3.5 MHz channel bandwidth. Peak/Avg = 10.3dB @ 0.01% probability on CCDF, 2% EVM.

It can be observed from Table 2 that there is a lot of margin with respect to thermal management of Nitronex's current plastic packaged parts for WiMAX applications. This table only utilizes the $\theta_{j\text{-}c}$ thermal resistance contribution, but it gives the engineer an idea as to the margin in T_J that is available considering all the other thermal resistance contributions shown in figures 2 and 3. The design engineer can use these calculations to consider tradeoffs from the added contributions to $\theta_{j\text{-}a}$ with respect to thermal grease, vias or coin/pedestals, etc.

4.4. Mounting Methods for PSOP2 Package: Via Farm vs. Cu Coin/Pedestal

Nitronex's current plastic parts are built using the PSOP2 RF Transistor package. The PSOP2 package utilizes conventional lead-frame and plastic overmolding technology and has a slug/paddle on the bottom of the package to provide the primary heat removal path. Maximum thermal management is achieved when the heat slug is properly attached to a heat spreader and external heat sink. This section first presents the design and results for a via farm approach, then presents the design and results of Cu coin/pedestal approach.

4.4.1. Via Farm Thermal Design Approach

PCB materials typically are not very thermally conductive. For lower power requirements the PSOP2 can be mounted directly on the PCB with via structures and still maintain proper thermal and grounding performance. The number of vias, their size and orientation are application specific so thermal and electrical modeling and evaluations should be performed to determine if the solution is adequate for the proposed application.

Figure 4 shows a metal filed via structure and solder pad layout utilized for the NPTB00004. The via holes are ~0.012" (0.33mm) in diameter with 2 ounce Cu plating. It is recommended that thicker ounce Cu plating be utilized to plug the via holes. This prevents solder from wicking into the vias and voids from forming underneath the source slug when the device is soldered to the PCB. The distance between the via hole centers is maintained at 0.025". To ensure a good thermal path between the PCB and the heat sink it is recommended to incorporate two mounting holes for #2-56 (M2) screws. Using a torque of 2.5 inch-pounds (0.29 N-m) promotes the proper seating of the metal heat sink to the back of the PCB. Results of infrared imaging measurements on this via farm design are presented below in section 4.4.1.1.

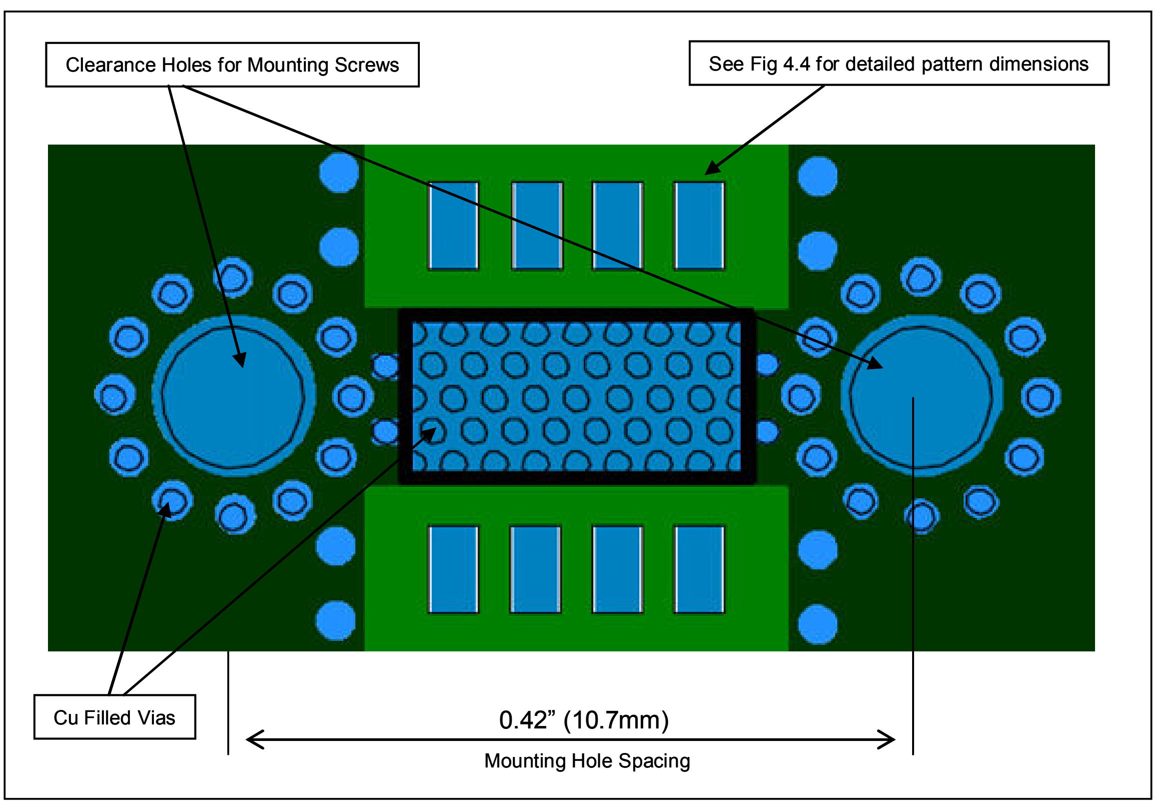

Figure 4. Optimized Via Pattern for PSOP2 NPTB00004

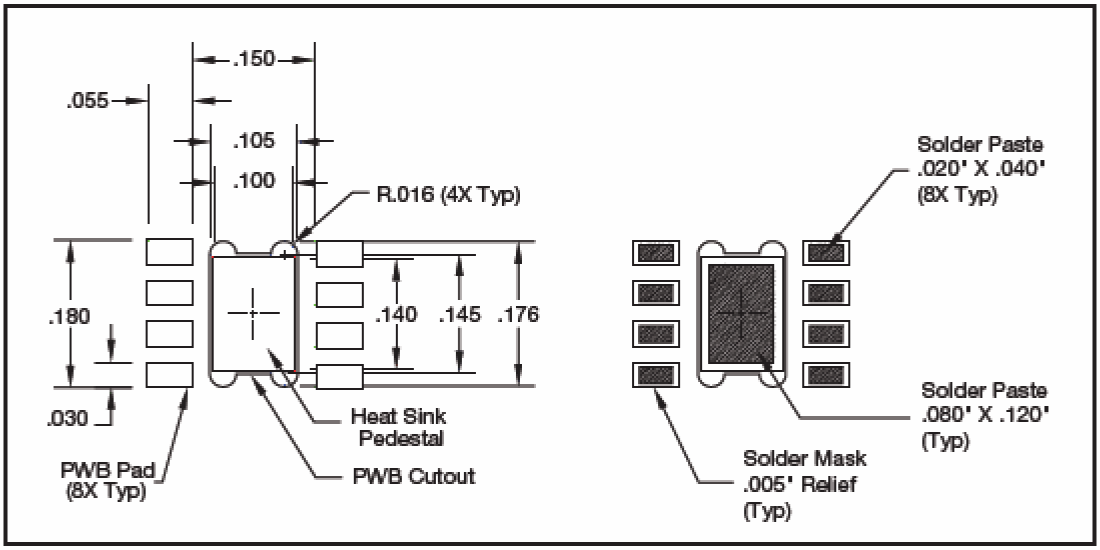

Figure 5. Solder Paste PSOP2 Footprint Pattern (5mil screen)

4.4.1.1. Via Farm Thermal Scan Results of the NPTB00004

Infrared thermal imaging measurements were made on an NPTB00004 application board which utilized the via farm design shown in Figure 6. Measurements were taken under DC Bias with total power dissipations of 1.4, 2.8 and 4.2W with a baseplate temperature of 80°C. The following experiments were conducted to achieve worse case junction temperatures of 200°C+. These are not recommended temperatures of operation.

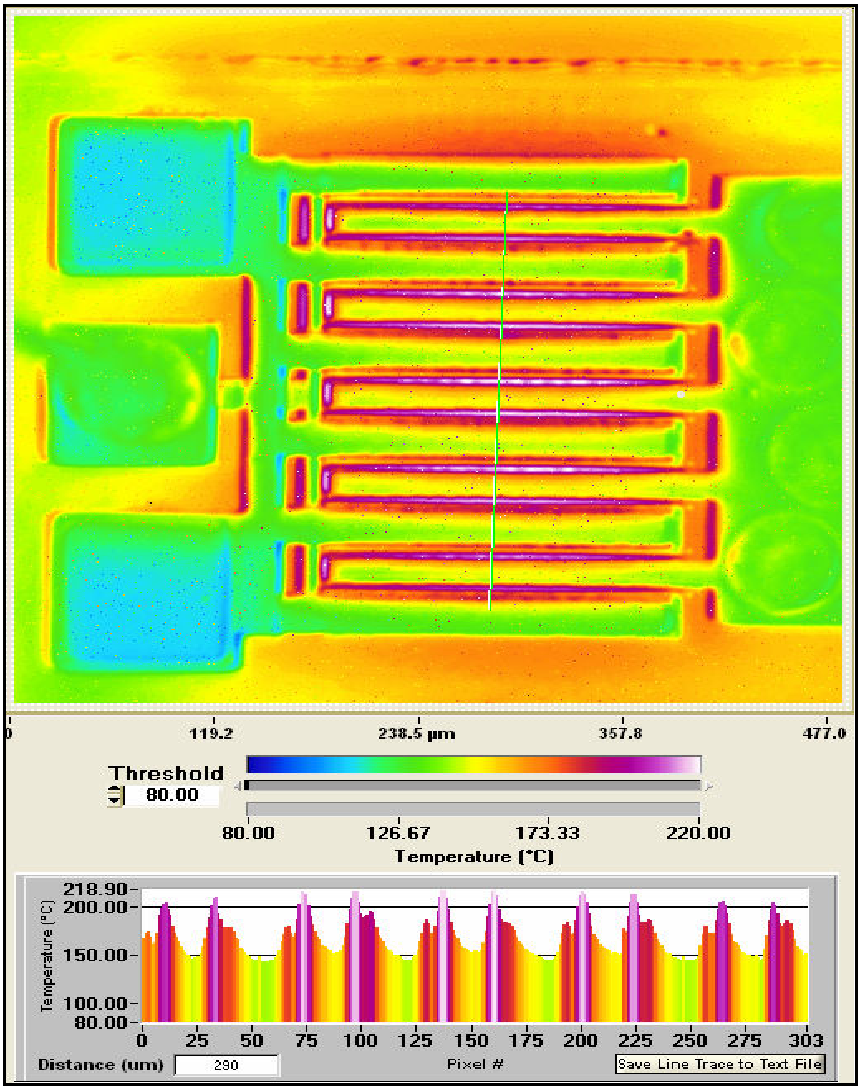

Figure 6. Quantum Focus Infrascope II Results of the Thermal Via Design

Table 3. Thermal Via Thermal Scan Results

V_{DS} (V)	I_{DS} (mA)	P_{DISS} (W)	T_J (°C)	θ_{j-a} (Ω)
28	50	1.4	119	27.9
28	100	2.8	162	29.3
28	150	4.2	219	33.1

4.4.2. Cu Coin/Pedestal Thermal Design Approach

The PSOP2 has a slug/paddle on the bottom of the package to provide the primary heat removal path. Maximum thermal performance may be achieved when the heat slug is properly attached to the PCB and external heat sink. This section presents the designs and results for a Cu Coin and discusses a pedestal approach for the thermal management solution.

Figure 7 shows the layout to be used to incorporate a pedestal thermal solution. For the pedestal approach the PSOP2 is soldered directly to the heat sink and alleviates the additional thermal resistance introduced by a thermal conductive grease layer, as well as the need to incorporate mounting screws to guarantee good thermal/electrical connection between the Cu coin and the heat sink. The top of the pedestal needs to be flush with the top of the PCB. (this prevents damage/stress on the PSOP2 package leads)

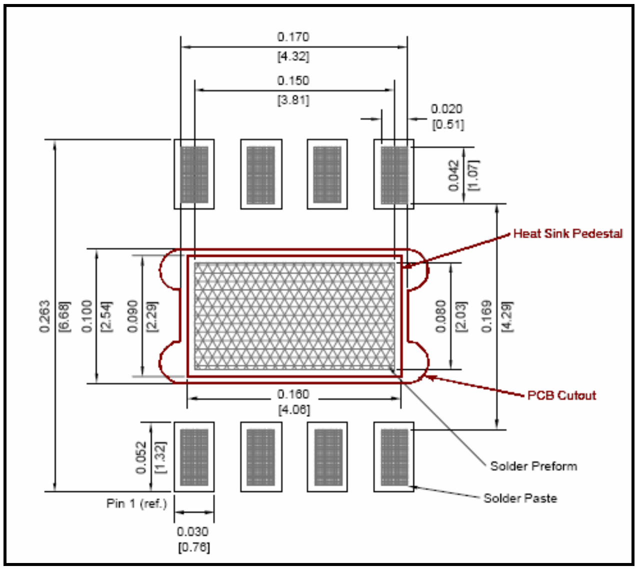

Figure 7. Cu Pedestal Thermal Design Drawing

Figure 8 shows the layout to be used for a Cu coin thermal solution. For this solution the PCB needs to have a cutout and the top of the coin needs to be flush with the top of the PCB.

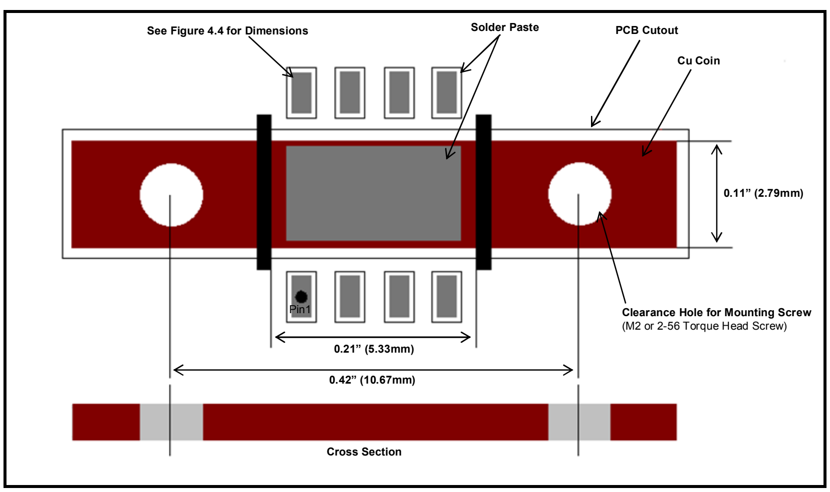

Figure 8. Cu Coin Thermal Design Drawing

4.4.2.1. Cu Coin Thermal Scan Results of the NPTB00004

Infrared thermal imaging measurements were made on an NPTB00004 which was soldered to a Cu coin. CircuitWorks CW7100 thermal grease was used to provide the heat conduction path between the bottom of the coin and the heat sink. Measurements were taken under DC Bias with total power dissipations of 1.4, 2.8 and 4.2W with a base plate temperature of 80°C, and are shown below in Figure 9.

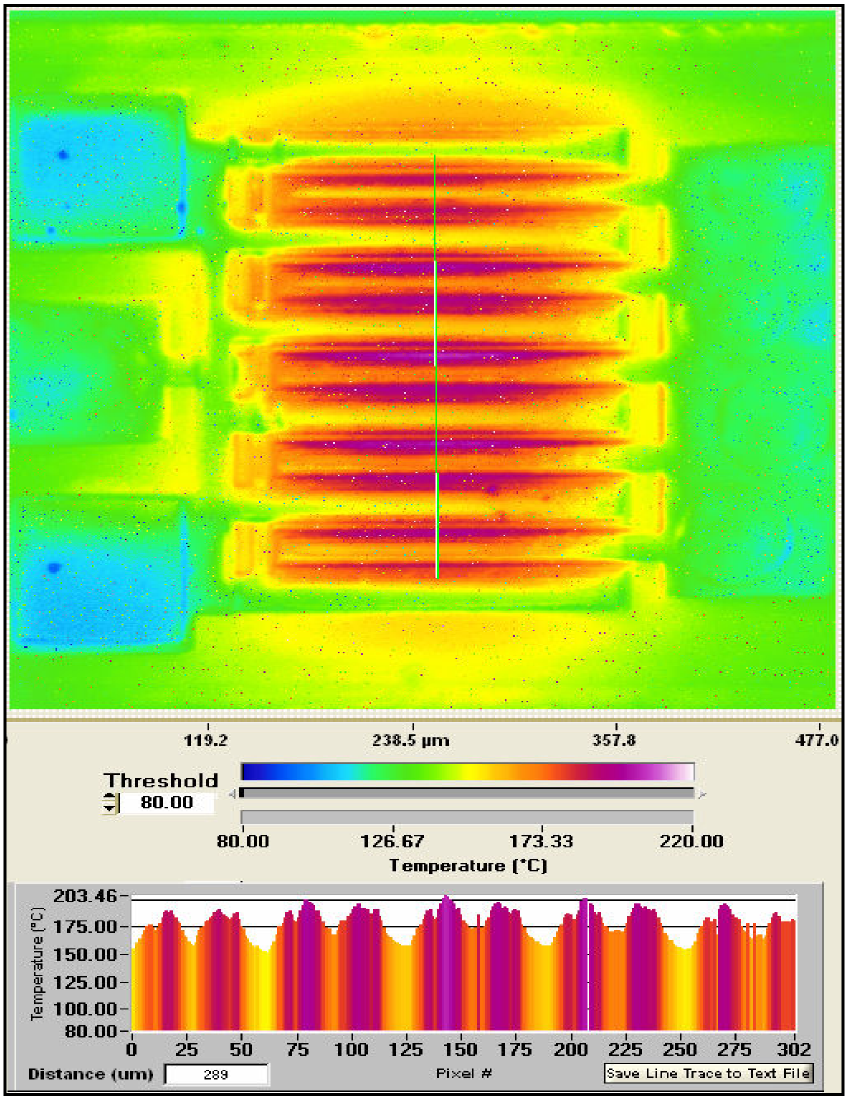

Figure 9. Quantum Focus Infrascope II Results of the Cu Coin Thermal Design

Table 4. Cu Coin Thermal Scan Results

V_{DS} (V)	I_{DS} (mA)	P_{DISS} (W)	T_J (°C)	θ_{j-a} (Ω)
28	50	1.4	116	25.7
28	100	2.8	155	26.8
28	150	4.2	203	29.3

4.4.3. Cu Coin vs. Thermal Via Thermal Scan Results Comparison

Table 5. Infrascope II Results Comparison Table

V_{DS} (V)	I_{DS} (mA)	P_{DISS} (W)	Cu Coin T_J (°C)	Via Farm T_J (°C)	Δ T_J (°C)
28	50	1.4	116	119	3
28	100	2.8	155	162	7
28	150	4.2	203	219	16

From Table 5 it can be observed that the use of thermal vias increases the junction temperature by 3-16°C over the Cu coin approach. Table 6 below enumerates out the thermal resistances shown previously in figures 4.1 and 4.2. It can also be noted that the junction temperatures have exceeded the desired 200°C; part of this is due to the thermal grease contribution represented as θc-p. (note that the thermal grease is located between the PCB and heat sink and between the Cu Coin and heat sink, Figures 4.1 and 4.2 have this thermal resistance contribution included in with θc-p which also has the resistance contributions from the solder connecting the part to the coin or PCB.) θb-a is the other main contributor to the higher junction temperatures that were measured. The θb-a contribution can be minimized with the proper choice of heat sinking material, ideally Cu would be best choice, this application utilized a nickel plated aluminum block.

Table 6. Thermal Resistance Calculations of Infrascope II Results for Cu Coin and Thermal Via Designs

	Device	Pout (W)	Gain (dB)	Drain Efficiency (%)	θ_{j-a}	θ_{j-c}	θ_{c-p}	θ_{p-b}	θ_{b-a}	Pdiss (W)	ΔT (°C)	Tbase (°C)	T_J (°C)
PCB with Cu Coin	NPTB00004	4.8	16.3	55	30.00	26.00	0.50	0.00	3.50	4.1	123.6	80	**203.6**
PCB with Via Farm	NPTB00004	4.8	16.3	55	33.80	26.00	0.50	3.80	3.50	4.1	139.3	80	**219.3**

The designer needs to take into account the contribution of θp-b of the thermal via approach, where as for the Cu coin approach this contribution is negligible. For higher power applications where there is less margin the thermal via approach can be ruled out rather quickly as a thermal solution based on the added thermal resistance contribution of the PCB. Figure 10 shows how the junction temperatures track with the two thermal designs over dissipated power.

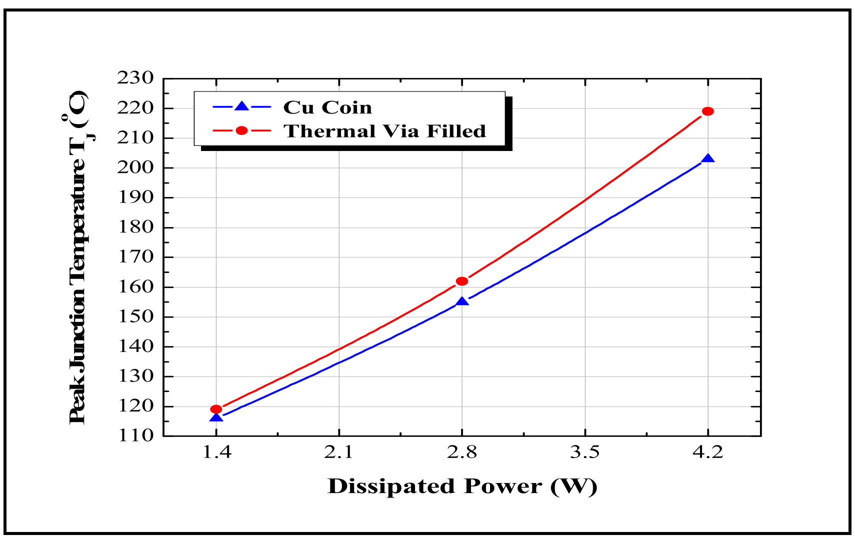

Figure 10. Infrascope II Thermal Scan Results Comparison Chart

4.4.4. Via Farm Simulations: Via Spacing, Via Diameter, Via Plating, PCB thickness

Section 4.4.2.2 presented measured thermal performance results of the thermal via design.(defined in 4.4.1) It was observed that the added contribution of θb-a and θc-p was enough to cause the junction temperature to exceed 200°C. The thermal via design geometry that was used for these simulations is shown below in Figure 11. This section will present simulated results observed when varying via size, via density, PCB thickness and via plating thickness. The following simulations were conducted to achieve worse case junction temperatures of 200°C+. These are not recommended temperatures of operation, the results are presented to show thermal trends of which to consider when finalizing a thermal design.

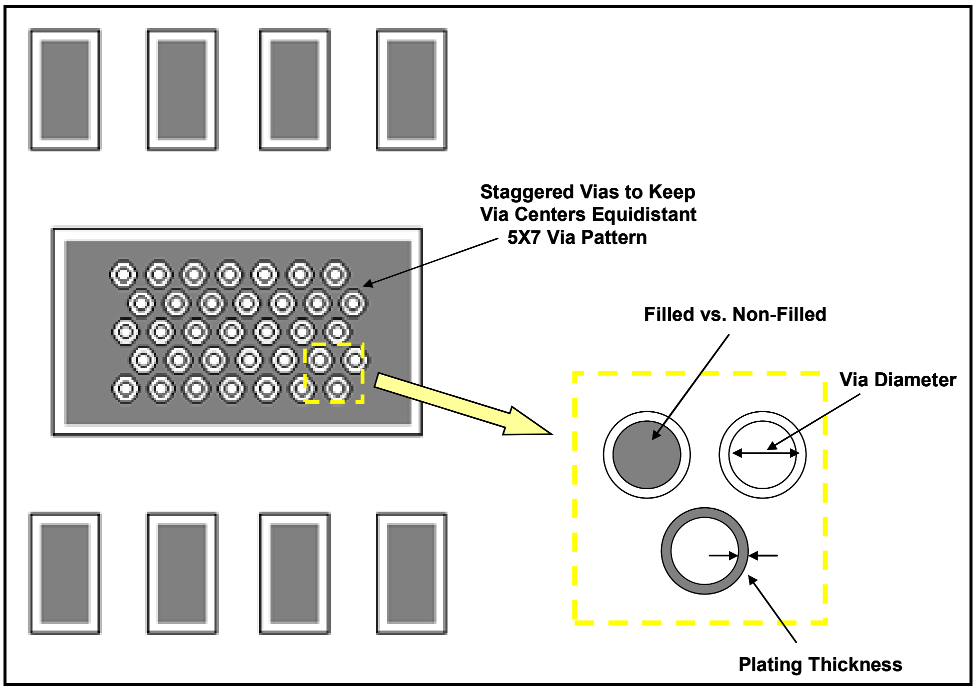

Figure 11. Thermal Via Simulation Geometry

A 5 by 7 array of 0.33mm diameter thermal vias was modeled with the following assumptions:

- The heat source is provided from the 2mm x 3mm source slug of the package part.
- The bottom surface of the PCB is an isothermal boundary
- Via diameter, Via Density in X/Y, PCB Thickness, and Via Plating thickness are the parameterized dimensions.
- The PCB material, Rodgers RO4350
- The $\theta_{c\text{-}p}$ of the thermal grease for this simulation is assumed constant
- The baseplate/heat sink is maintained at 85°C. Environment definition is shown below in Figure 12

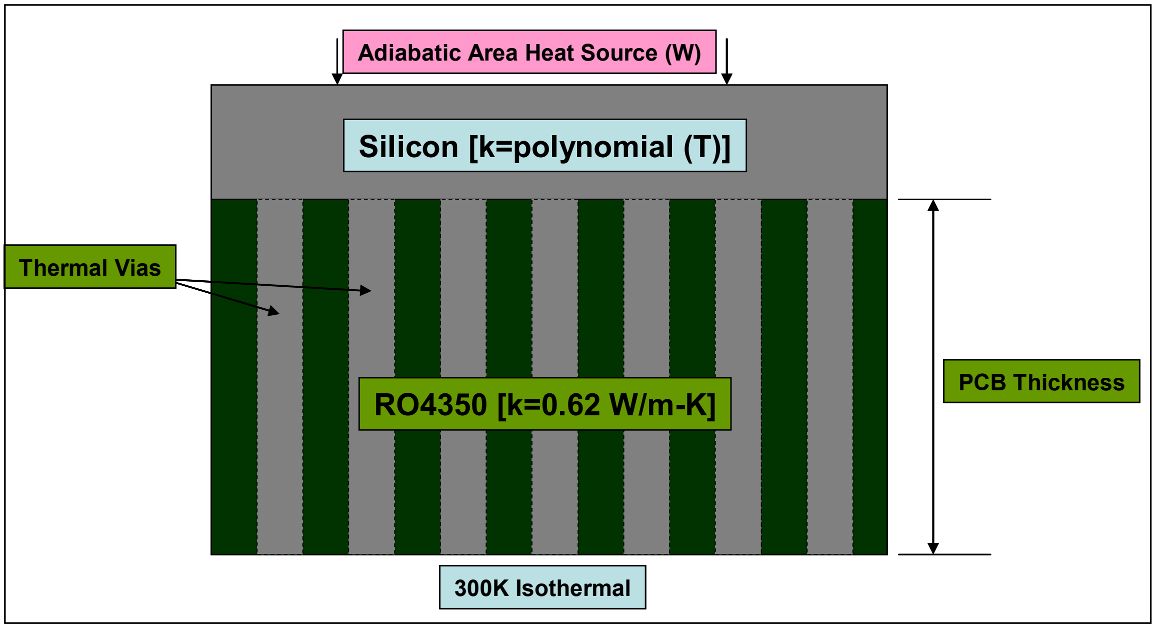

Figure 12. Environmental Variable Setup

4.4.4.1. Simulated Via Plating Thickness Study

This section presents the simulated thermal trends associated with increasing the via plating thickness.

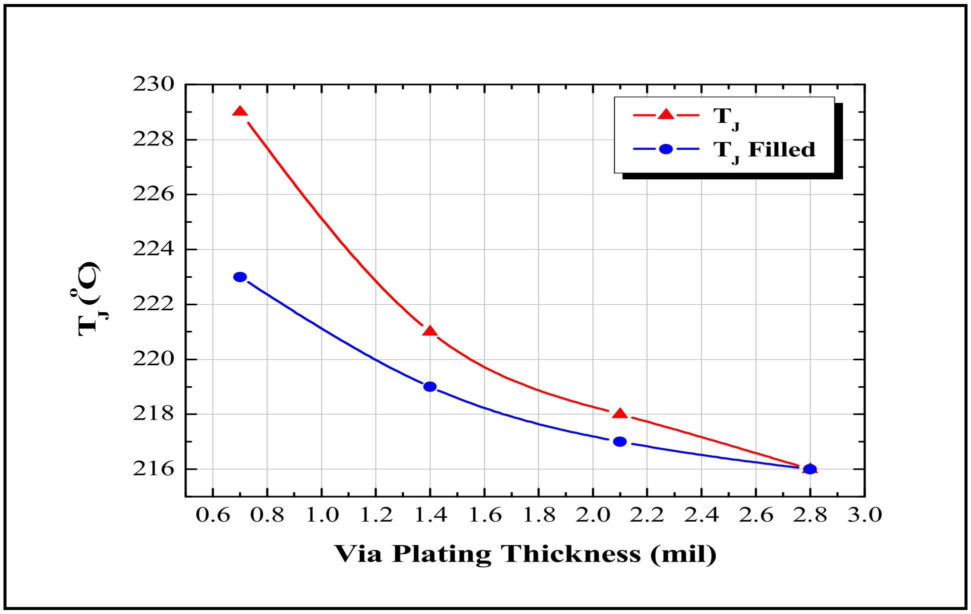

Figure 13. Simulated Via Plating Thickness Results

Table 7. Simulated Via Plating Thickness Results

Plating Thickness (mil)	Simulated TJ (°C)	Simulated TJ (°C) Filled *
0.7	229	223
1.4	221	219
2.1	218	217
2.8	**216**	**216**

The following observations can be made about the simulated results shown in Figure 13 and Table 7:

The difference in performance between a filled via and plated non-filled via decreases as the plating thickness increases (the plating eventually fills up the via)

The junction temperature decreases as the via plating thickness increases.

4.4.4.2.Simulated Via Diameter Study

This section presents the simulated thermal trends associated with increasing the via diameter.

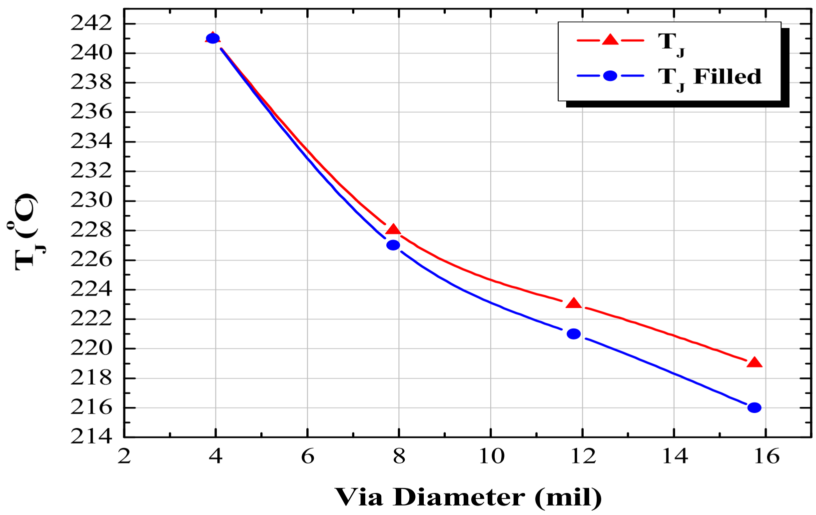

Figure 14. Simulated Via Diameter Results

Table 8. Simulated Via Diameter Results

Diameter (mil)	Simulated TJ (°C)	Simulated TJ (°C) Filled *
4	241	241
8	228	227
12	223	221
16	**219**	**216**

PCB Thickness=20mil, Via Plating=1.4mil

The following observations can be made of the simulated results shown in Figure 14 and Table 8:

The junction temperature decreases as the via diameter increases.

Most of the thermal conduction path appears to be through the metallization of the via plating since there is only a 3°C/W improvement from unfilled to filled.

Larger vias improve the thermal conduction performance through the PCB.

4.4.4.3.Simulated PCB Thickness Study

This section presents the simulated thermal trends associated with increasing the PCB thickness.

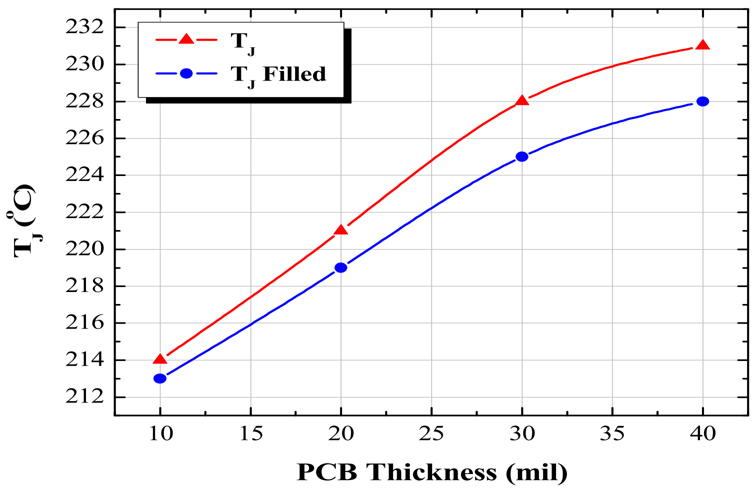

Figure 15. Simulated PCB Thickness Results

Table 9. Simulated Via Diameter Results

PCB Thickness (mil)	Simulated T_J (°C)	Simulated T_J (°C) Filled *
10	**214**	**213**
20	221	219
30	228	225
40	231	228

Via Diameter=.33mm, Via Plating=1.4mil

The following observations can be made from the simulated results shown in Figure 15 and Table 9:

The performance difference between a filled via and non-filled via increases as the PCB thickness increases.

The junction temperature increases as the PCB thickness increases.

The delta in thermal improvement between filled and non-filled vias is negligible as the PCB thickness gets thinner. However, vias should be filled to prevent voiding of solder underneath the source slug and to improve the thermal performance of the system.

4.4.4.4. Simulated Via Density Study

This section presents the simulated thermal trends associated with increasing the density of vias in a given area of PCB.

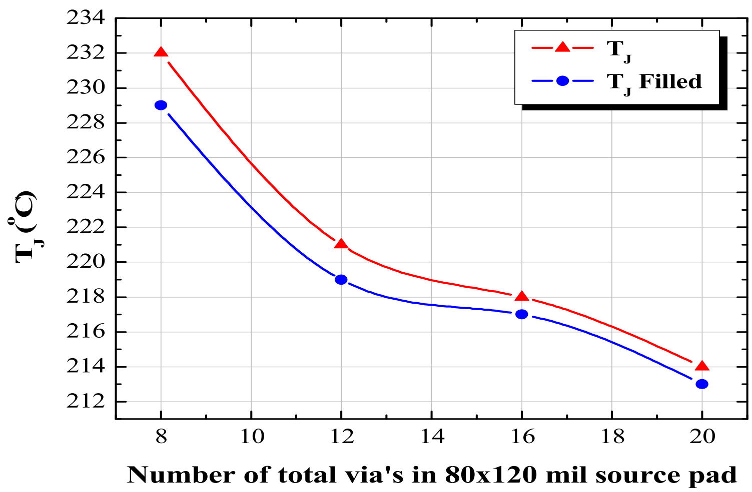

Figure 16. Simulated Via Density Results

Table 10. Simulated Via Density Results

Total # of Vias	# Vias in X	# Vias in Y	Pitch in X (mil)	Pitch in Y (mil)	Simulated TJ (°C)	Simulated TJ (°C) Filled *
8	3	5	48	38	232	229
12	5	7	25	25	221	219
16	7	9	15	18	218	217
20	9	11	13	14	214	213

Via Diameter=.33mm, PCB Thickness=20mil, Via Plating=1.4mil
Pitch is Set to Maintain Area of Source Slug (3mm X 5mm)

The following observations can be made from the simulated results shown in Figure 16 and Table 10:

- The performance difference between a filled via and non-filled via decreases as the via density increases.

The junction temperature decreases as the via density increases.

4.4.4.5.Optimum Simulated Thermal Via Solution

In the previous four sections simulated trends were presented for via plating thickness, via diameter, PCB thickness, and via density. This section presents simulated results utilizing the best solutions from each of the previously simulated variables.

Table 11. Optimum Simulated Thermal Solution Results

Diameter (mm)	Plating Thickness (mil)	PCB Thickness (mil)	#Vias in X/Y	Pitch in (X,Y)	Simulated TJ (C)	Simulated TJ (C) Filled *
0.4	2.8	10	(9,11)	(13,14)	**207**	**207**

The final result is a simulated junction temperature that is only 4°C higher than the results measured utilizing the Cu coin thermal design approach.

There is no difference between filled and non-filled vias. This is due to the fact that the plating is most likely filling the via.

5. Ceramic Air Cavity Thermal Design

5.1. Bolt-Down and Solder-Down Configuration Discussion

For very high power parts it is necessary to directly attach the package to the heat sink. Figure 17 illustrates this situation for a ceramic bolt down or solder down package. For pill packages the θ_{c-b} is relatively small in that the part is directly soldered to the heat sink. The bolt down package requires the use of thermal grease for the metal to metal interface, the quality of which can contribute to the overall thermal resistance. Results from a thermal grease study are given in section 5.2.

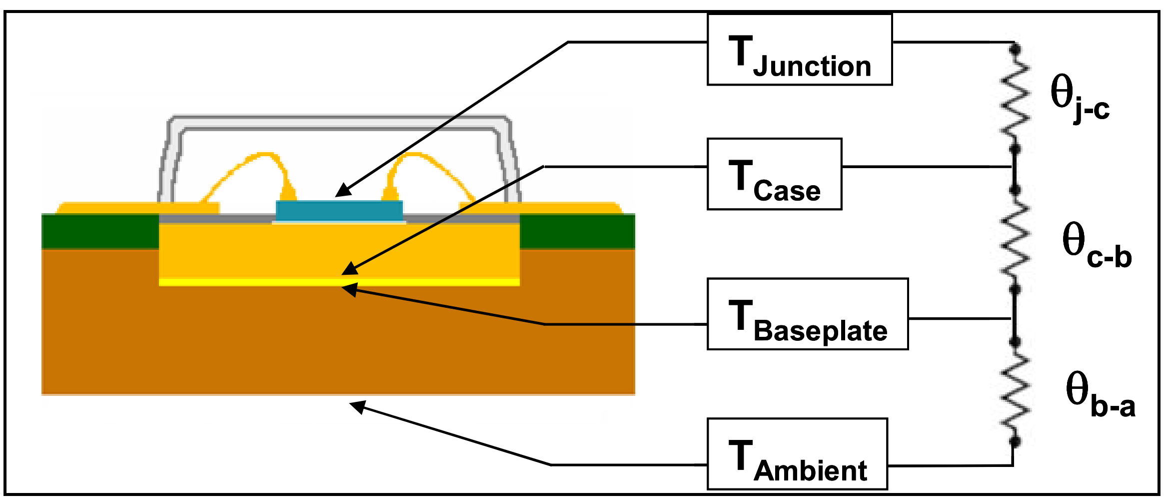

Figure 17. Thermal Stack of Ceramic Package

For a given power device and system requirement combination there are several fixed parameters that must be considered for worst-case conditions:

1. MTTF: determines maximum junction temperature
2. Worst case base plate temperature
3. θj-c as given by the device manufacturer
4. Maximum dissipated power as determined by bench measurements, simulations, experience.

From these parameters, the maximum allowable thermal resistance from the power transistor case to base plate temperature can be calculated as:

$$\theta_{j-b_{Max}} = \left(\frac{T_{J_{Max}} - T_{Baseplate_{Max}}}{P_{Diss_{Max}}} \right)$$

Where,

$$P_{Diss_{Max}} = V_d I_d - P_{Out} + P_{in}$$

$$T_{J_{Max}} = 180^{\circ} C$$ (See section 3.2)

$$T_{Ambient_{Max}}$$ (Determined by system specifications)

$$\theta_{c-b_{Max}} = \theta_{j-b_{Max}} - \theta_{j-c}$$

Section 5.3 presents some thermal calculations on Nitronex's current ceramic packaged product offering.

5.2. Thermal Grease Study for Mounting Bolt Down Packages to Cu Heat Sinks

The quality of the thermal grease interface between heat sinks and bolt down packages is another component of the thermal management system that needs to be considered for the optimum transfer of dissipated heat to the cooling medium. This section presents the data from an investigation into three different thermal grease compounds: Circuit Works' Silver Conductive Thermal Grease (CW7100), the standard non-conductive white thermal grease (RS) and Arctic Silver5(AS5*).

Test Setup: Two NPT35050 devices were used. The thermal grease was applied between the bolt down package and the application board heat sink block. The heat sink block and device were cleaned with alcohol wipes before the application of each alternative thermal grease. The devices were DC biased, with no RF Power and all of the DC power was dissipated off as heat. Three different power levels were measured (22W, 39W and 56W). The results were obtained with a Quantum Focus Infrascope II Thermal Imaging System, and are shown below in Table 12.

The CircuitWorks CW7100 was slightly better than the standard non-conductive white thermal grease (RS) at the lowest temperature and was increasingly more effective as the power density was increased. At the highest dissipated power the CW7100 yielded a 7-22% reduction in calculated Rth versus the standard RS grease, this amounted to a 8 to 26 °C reduction in junction temperature, T_J. The Arctic Silver5(AS5*) was measured to have poor thermal performance in this study, measuring 15-28% worse than the standard RS grease.

As can be observed from these test results, the thermal grease selection is another aspect of the thermal management system that shouldn't be overlooked. The selection of the wrong grease in this study showed the ability to cause the junction temperature to exceed the acceptable limits, thus degrading component performance and lifetime.

Table 12. Quantum Focus Imaging Results on NPT35050 Thermal Grease Experiment

Thermal Grease Study Results										
NPT35050 DUT	Thermal Grease Type	Case Temperature (°C)			Junction Temperature (°C)			Calculated Rth (°C/W)		
		P_D=22W	P_D=39W	P_D=56W	P_D=22W	P_D=39W	P_D=56W	P_D=22W	P_D=39W	P_D=56W
9829	RS White Grease	86.5	91.8	97.5	123	163	211	1.64	1.81	2.02
9829	CW7100	86.6	92.1	97.6	122	162	203	1.59	1.78	1.88
9829	Arctic Silver5	98.4	95.4	102.3	140	194	247	1.86	2.51	2.58
9842	RS White Grease	86.6	92.2	97.8	124	166	211	1.68	1.88	2.02
9842	CW7100	85.7	90.8	95.9	116	150	185	1.36	1.51	1.59
9842	Arctic Silver5	87.5	93.9	99.9	133	182	230	2.04	2.25	2.32

5.3. Nitronex Ceramic Packaged Parts

This section presents some thermal calculations for Nitronex's current ceramic packaged product offering for CW and WiMAX applications.

5.3.1. CW Applications

Table 13 presents thermal calculations for Nitronex ceramic parts intended for CW Applications. Typical thermal resistance, CW output power, gain and drain efficiency values were taken from the latest product datasheets. Calculations for ∆T and T_J were made using equations from section 3.1 and 3.2.

The following assumptions were made:

- The baseplate temperature is maintained at 70°C
- The performance data is taken at 2.5GHz, except for NPT35050 which is at 3.5GHz.
- Data utilized for gain, Pout and drain efficiency was taken at 25°C. Calculations are optimistic because they do not take into account effects of temperature on Pout, gain and drain efficiency.

Table 13. Nitronex Ceramic Part Thermal Calculation Table for CW Applications

Device	Pout (W)	Gain (dB)	Drain Efficiency (%)	θ_{j-c}	Pdiss	∆T (°C)	Tbase (°C)	T_J (°C)
NPTB00025	25	10.5	65	5.25	15.7	82.4	70	152.4
NPT35050	32	11.0	36	1.95	58.7	114.4	70	184.4
NPTB00050	50	10.0	62	3.20	35.6	114.1	70	184.1
NPT25100	90	13.5	62	1.75	59.2	103.6	70	173.6

Typically designers are asked to maintain MTTF lifetimes of 10^6 hours. Figure 3.1 shows that this equates to keeping junction temperatures lower than ~180°C. Calculations in Table 13 show that there is some margin in baseplate temperatures for the NPTB00025 and NPT25100 to maintain the desired MTTF.

The designer in this use case needs to utilize direct heat sinking to the source/flange of these parts. The bolt down packages includes the thermal resistance contribution of the conductive grease described in section 5.1. Earless parts that are directly soldered to the heat sinks add a negligible amount of thermal resistance.

5.3.2. WiMAX Applications

Table 14 presents thermal calculations of Nitronex ceramic parts for WiMAX applications. Typical thermal resistance, output power, gain and drain efficiency values were taken from the latest product datasheets. Calculations for delta T and the junction temperatures were calculated using equations from sections 3.1 and 3.2.

- The baseplate temperature is maintained at 85°C
- The performance data is taken at 2.5GHz, except for NPT35050 which is at 3.5GHz.
- Data utilized for gain, Pout and drain efficiency was taken at 25°C. Calculations are optimistic because they do not take into account effects of temperature on Pout, gain and drain efficiency.
- EVM does not exceed 2%

Table 14. Nitronex Ceramic Part Thermal Calculation Table for WiMAX Applications

Device	Pout (W)	Gain (dB)	Drain Efficiency	$\theta_{j\text{-}c}$ (Ω)	Pdiss (W)	ΔT (°C)	Tbase (°C)	T_J (°C)
NPT35050 [2]	7	12.0	18	1.95	30.0	58.5	85	143.5
NPT25100 [1]	10	16.5	26	1.75	28.7	50.2	85	135.2

Note 1: Single carrier OFDM waveform 64-QAM 3/4, 8 burst, continuous frame data, 10 MHz channel bandwidth. Peak/Avg = 10.3dB @ 0.01% probability on CCDF, 2% EVM.
Note 2: Single carrier OFDM waveform 64-QAM 3/4, 8 burst, 20ms frame, 15ms frame data, 3.5 MHz channel bandwidth. Peak/Avg = 10.3dB @ 0.01% probability on CCDF, 2% EVM.

It can be observed from Table 14 that there is a lot of margin with respect to thermal management of Nitronex's current ceramic packaged parts for WiMAX applications.