

APPLICATION NOTE

Suggested PCB Land Pattern Designs for Leaded and Leadless Packages, and Surface Mount Guidelines for Leadless Packages

Introduction

This Application Note provides sample PCB land pattern dimensions for a variety of leaded and leadless packages. These drawings conform with the Surface Mount Design and Land Pattern Standard (IPC-SM-782) as published by the Institute for Interconnecting and Packaging Electronic Circuits (IPC).

Table 1 lists the land pattern drawings in this document together with their respective Figure numbers. These drawings are for reference purposes only. Skyworks recommends contacting the company doing the component mounting and soldering for more information related to actual land patterns (additional dimensions, etc.).

Surface Mount Guidelines for Leadless Packages

Skyworks plastic encapsulated leadless style packages are being offered on a number of products to reduce size and weight, and to improve application performance. These packages are gaining acceptance in the industry and are often referred to by such names as Quad Flat No-Lead (QFN), Leadless Plastic Chip Carrier (LPCC), Dual Flat No-Lead (DFN), et. al. All of them conform to JEDEC outline MO-220.

As indicated in Figure 1, leadless packages use perimeter lands on the bottom of the package to provide contact with the PCB. These packages also have an exposed paddle on the bottom to provide a stable ground for optimum electrical performance of switches and attenuators, and an efficient heat path for thermal performance of amplifier products.

Table 1. PCB Land Pattern Drawings Included in This Application Note

Package Type	Figure #	Package Type	Figure #
LGA	4	SOD-323	20
LGA-8, LGA-315 (4.9 x 3.2 mm)	5	SOIC (8-Lead)	21
LPCC-307 (16-Lead, 4 x 4 mm, Surface Mount)	6	SOIC (8-Lead, Narrow Body)	22
MSOP-8	7	SOIC (14-Lead, Narrow Body)	23
MSOP-10	8	SOIC (16-Lead, Narrow Body)	24
QFN (12-Lead, 3 x 3 mm)	9	SOIC (16-Lead, Wide Body)	25
QFN (6-Lead)	10	SOIC (28-Lead, Wide Body)	26
QFN (20-Lead, 4 x 4 mm)	11	SOT-5, SOT-6	27
QFN (20-Lead, 4 x 4 mm, 2.1 mm Paddle)	12	SOT-23 (3-Lead)	28
QFN-306 (16-Lead, 4 x 4 mm)	13	SOT-143	29
QFN-310, QFN-364 (32-Lead, 5 x 5 mm, Surface Mount)	14	SOT-666	30
QFN-349 (8-Lead, 2 x 2 mm)	15	SSOP (8-Lead, 5.3 mm)	31
QFN-350 (16-Lead, 3 x 3 mm)	16	SSOP (16-Lead)	32
SC-70	17	SSOP (20-Lead)	33
SC-70 (6-Lead), SC-88	18	TSSOP (16-Lead, Exposed Pad)	34
SC-79	19		

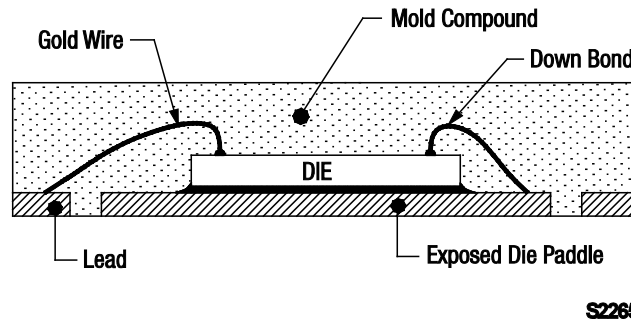


Figure 1. Package Cross Section

PCB Design Guidelines

For a lead/terminal solder pad design, it is recommended to use a Non-Solder Mask Defined (NSMD) approach. However, a small amount of solder mask should remain between the pads to avoid solder bridging between terminals. The PCB land width should match package pad width. The PCB land length should be 0.1 mm greater than the package pad length, with the extra area on the outside of the package (see Figure 7 for example).

The ground pad on the PCB should match the size of the exposed paddle of the package and should be Solder Mask Defined (SMD). The solder mask opening should overlap the edges of the PCB ground pad by 0.065 mm on all four sides. The recommended design gap between the PCB ground pad and land pad is 0.15 mm minimum to avoid solder bridging and shorting. When space is available, a gap of 0.25 mm or more is preferred.

Plated through via holes in the PCB ground pad should be 0.33 mm in diameter and plugged. If via holes cannot be plugged, it is recommended to cap the vias on the backside of the board using solder mask material. This should allow the vias to be filled with solder during reflow.

Solder Mask Design

Two types of stencil designs are used for surface mounted packages:

1. SMD: Solder mask openings are smaller than metal pads.
2. NSMD: Solder mask openings larger than metal pads.

NSMD is recommended for the perimeter I/O land pad, which allows the solder to wrap around the sides of the metal pads on the board for a reliable solder joint.

Since the spacing between the ground pad and the land pads can be small, SMD is recommended for the ground pad to prevent solder bridging.

A stainless steel stencil, 0.125 to 0.150 mm (0.005 to 0.006 in) thick, is recommended for solder paste applications. For better paste release, the aperture walls should be trapezoidal and the corners rounded.

For the terminal land pads, the stencil opening should be 0.05 mm larger than the PCB land pad (0.025 mm in each direction).

For the ground pad area, it is recommended to screen the solder paste in an array of small openings rather than one large opening. The total (cumulative) area of all the openings should be approximately equal to 50 percent of the total ground pad area. This ensures good solder coverage with fewer voids (refer to Figure 2)

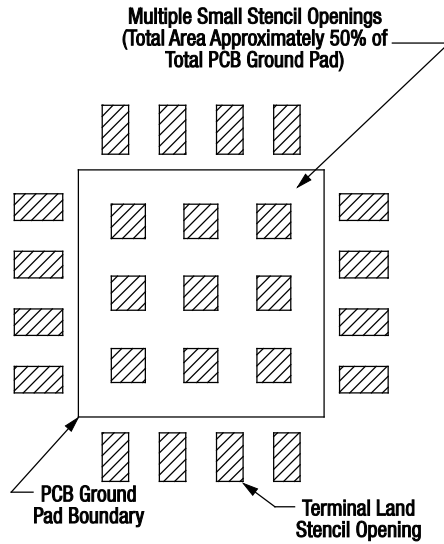
Solder Paste and Reflow Profile

Since leadless packages have a low stand-off height and small terminal pitch, a no-clean, type 3 solder paste and a convection/IR reflow are recommended.

Sn63 (63 percent Sn and 37 percent Pb) solder is preferred because it is a eutectic compound with a melting point of 183 °C. The reflow temperature in this case would be above 183 °C for 30 to 60 seconds, with a peak temperature of 205 to 210 °C.

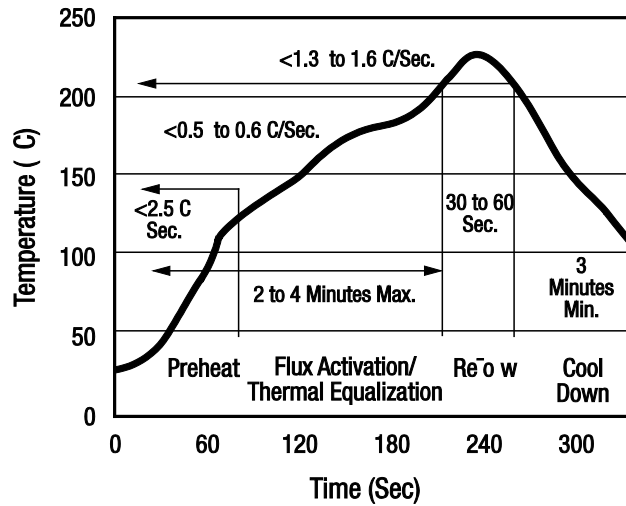
A Pb-free alloy may also be used. In the case of Sn/Ag or Sn/Ag/Cu, the melting points would be 221 °C and 217 °C, respectively. In this case, the profile would be above 221/217 °C for 30 to 90 seconds with a peak temperature of 235 to 245 °C. The maximum temperature should not exceed 245 °C.

A typical reflow profile is presented in Figure 3, which could be used as a starting point. The actual profile used depends on the thermal mass of the entire populated board and the solder compound used.



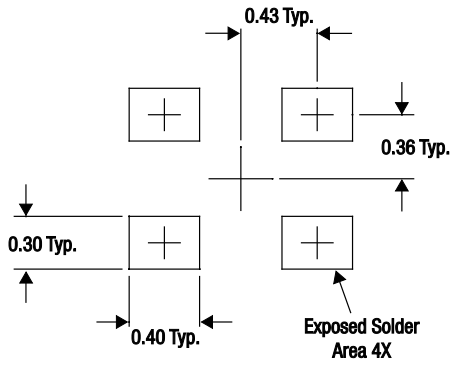
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Figure 2. Recommended Stencil Design



S2291

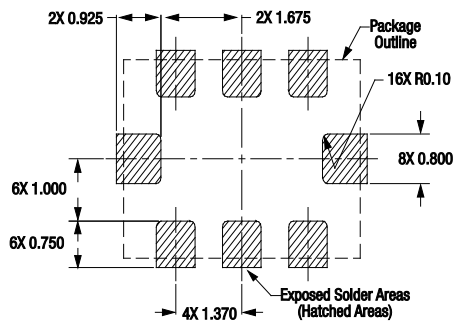
Figure 3. Typical Solder Reflow Profile



Note: Stencil aperture size should be 80% to 100% of the pad size on the board

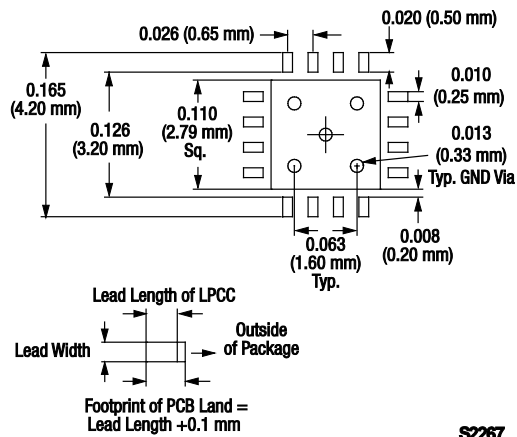
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Figure 4. Land Grid Array (LGA)



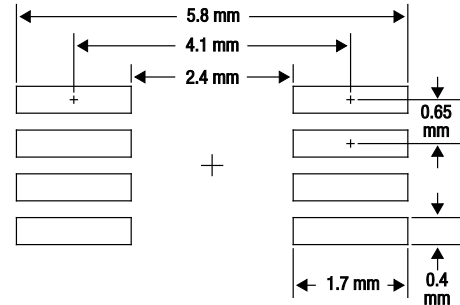
S2275

Figure 5. LGA-8, LGA-315 (4.9 x 3.2 mm)



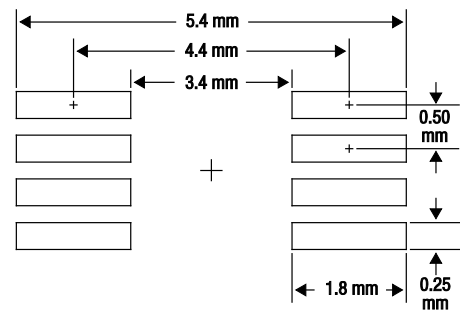
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Figure 6. LPCC-307 (16-Lead, 4 x 4 mm, Surface Mount)



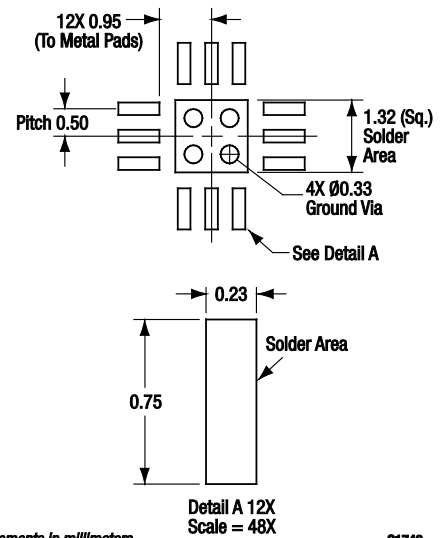
S2280

Figure 7. Micro Small Outline Package (MSOP-8)



S2289

Figure 8. MSOP-10



All measurements in millimeters

Detail A 12X Scale = 48X

S1748

Figure 9. QFN (12-Lead, 3 x 3 mm)

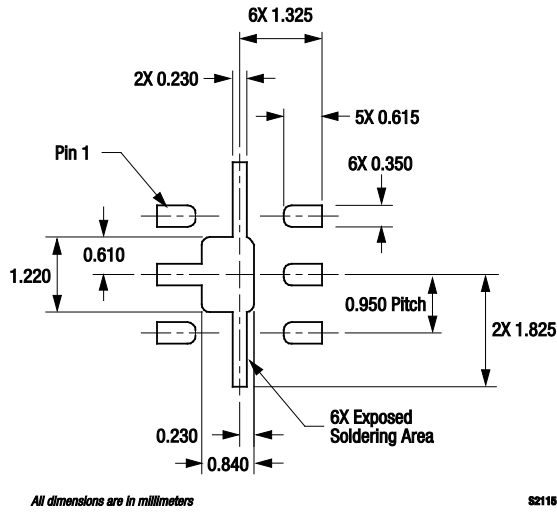


Figure 10. QFN (6-Lead)

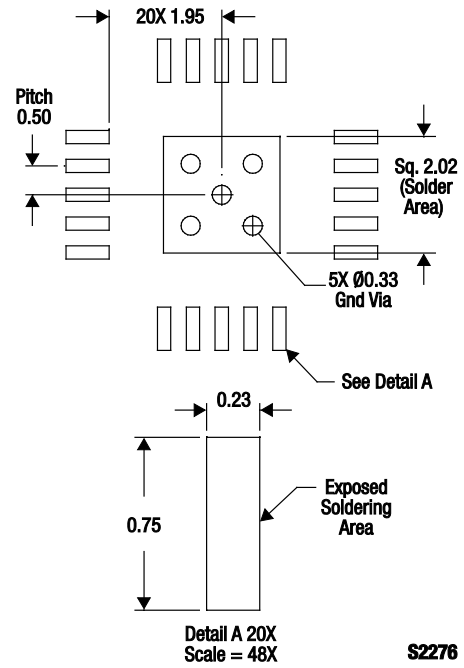


Figure 12. QFN (20-Lead, 4 x 4 mm, 2.1 mm Paddle)

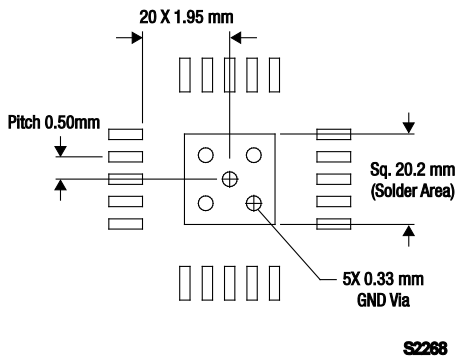


Figure 11. QFN (20-Lead, 4 x 4 mm)

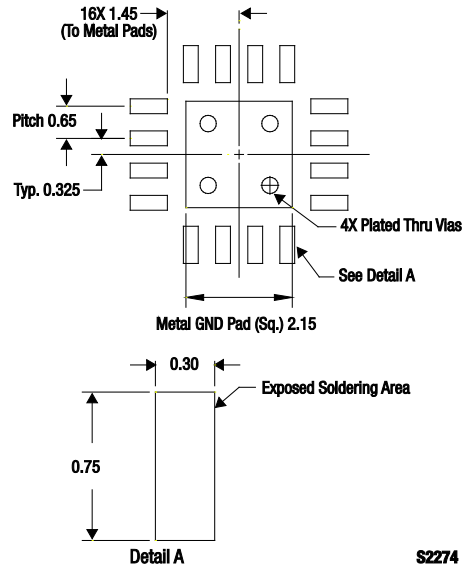


Figure 13. QFN-306 (16-Lead, 4 x 4 mm)

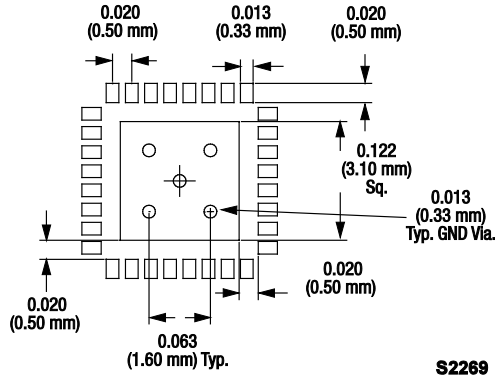


Figure 14. QFN-310, QFN-364 (32-Lead, 5 x 5 mm, Surface Mount)

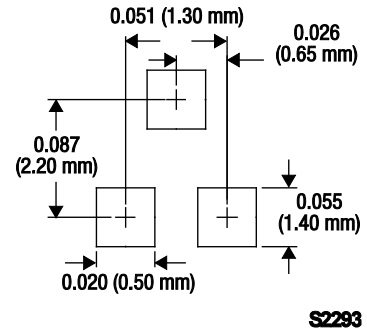


Figure 17. SC-70

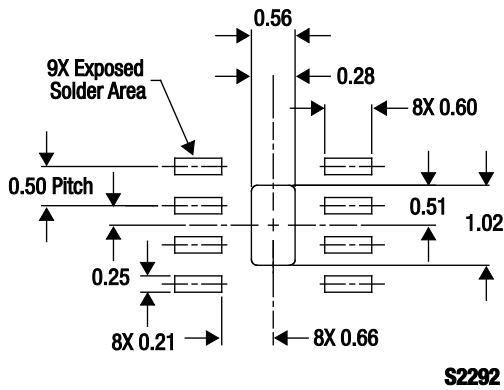


Figure 15. QFN-349 (8-Lead, 2 x 2 mm)

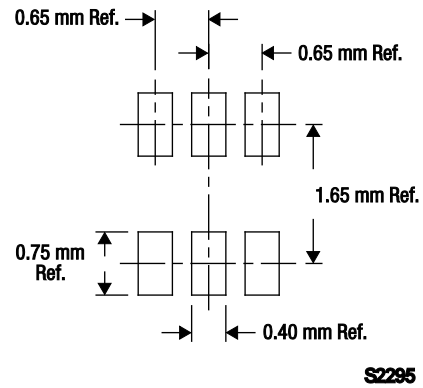


Figure 18. SC-70 (6-Lead), SC-88

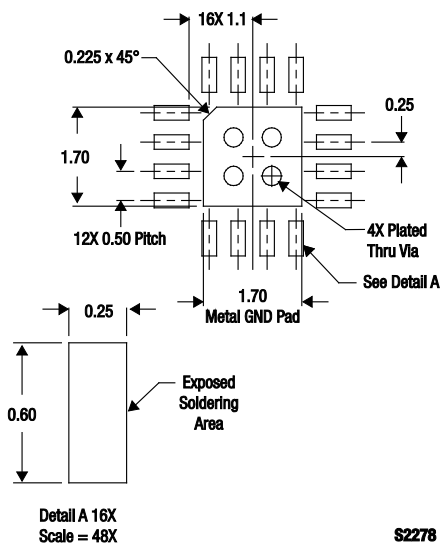


Figure 16. QFN-350 (16-Lead, 3 x 3 mm)

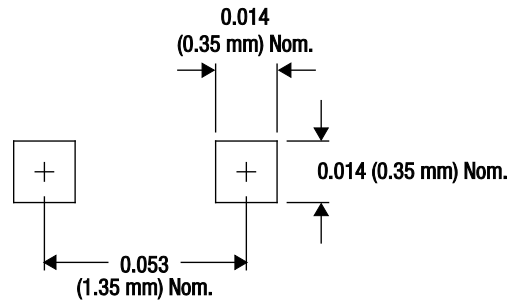


Figure 19. SC-79

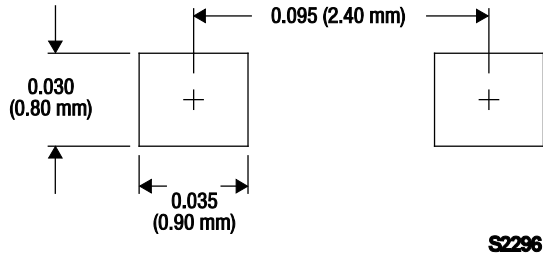


Figure 23. Small Outline Diode (SOD-323)

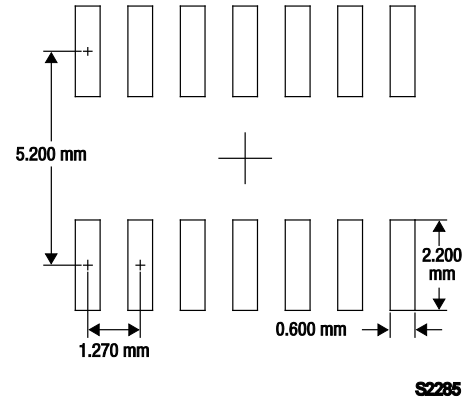


Figure 23. SOIC (14-Lead, Narrow Body)

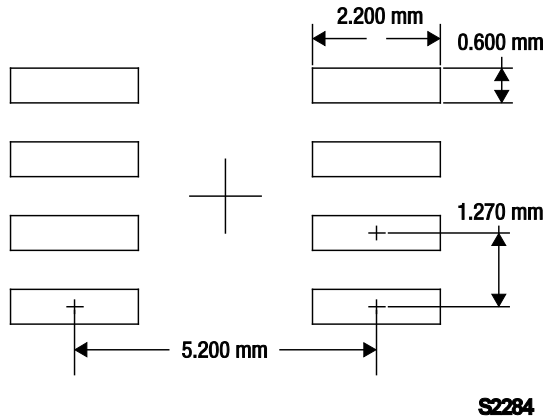


Figure 21. Small Outline Integrated Circuit (SOIC) (8-Lead)

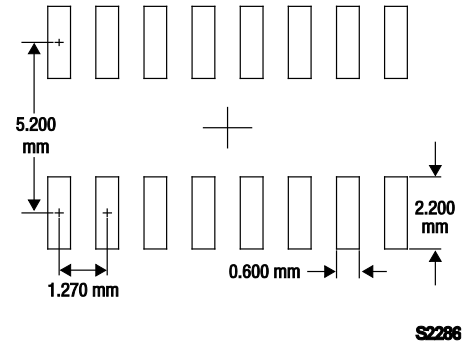


Figure 24. SOIC (16-Lead, Narrow Body)

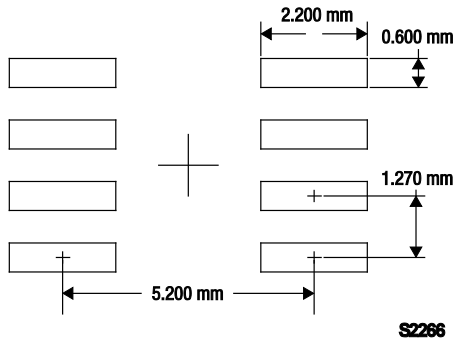


Figure 22. SOIC (8-Lead, Narrow Body)

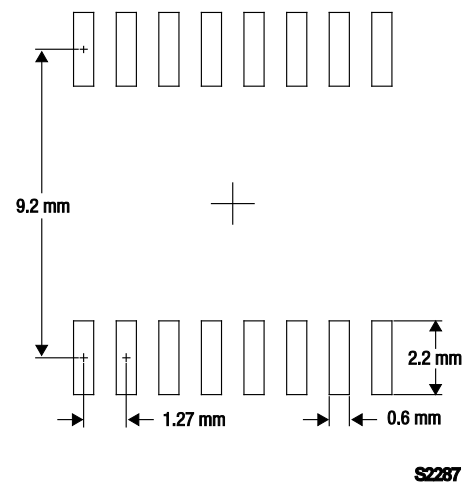


Figure 25. SOIC (16-Lead, Wide Body)

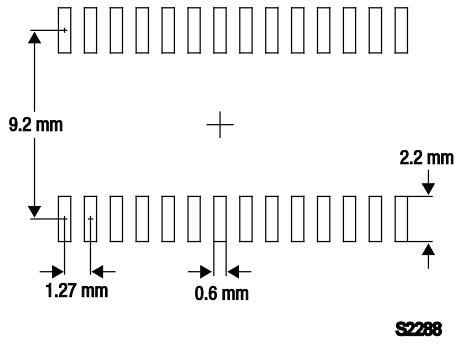


Figure 26. SOIC (28-Lead, Wide Body)

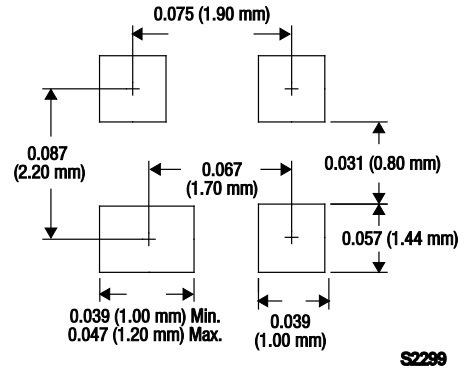


Figure 29. SOT-143

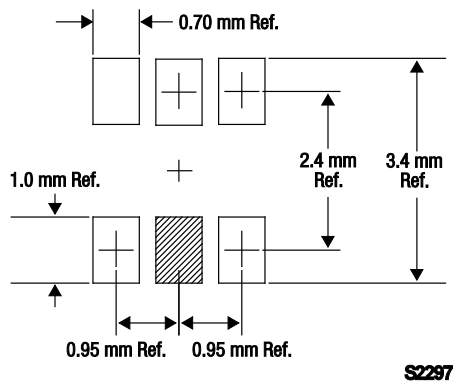


Figure 27. Small Outline Transistor (SOT-5, SOT-6)

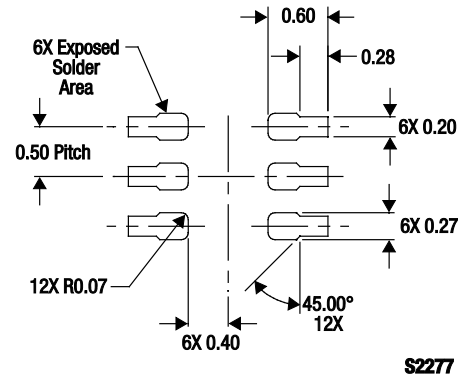


Figure 30. SOT-666

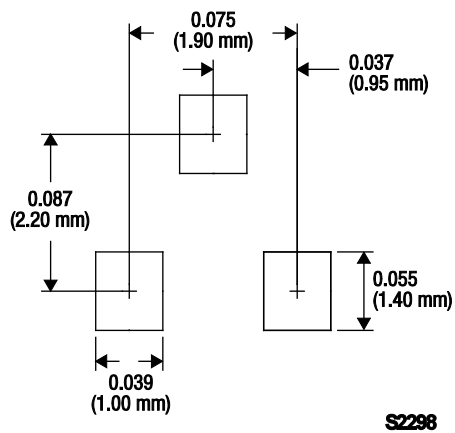


Figure 28. SOT-23 (3-Lead)

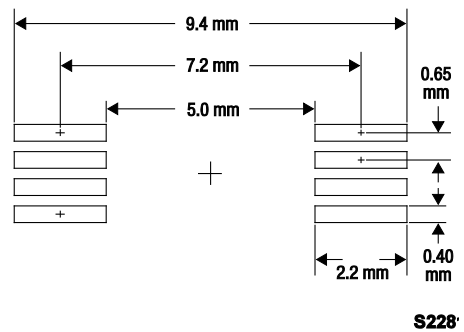


Figure 31. Small Shrink Outline Package (SSOP) (8-Lead, 5.3 mm)

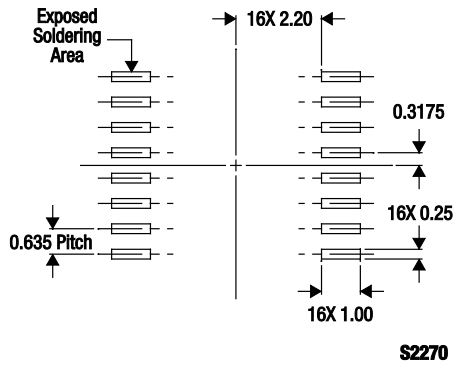


Figure 32. SSOP (16-Lead)

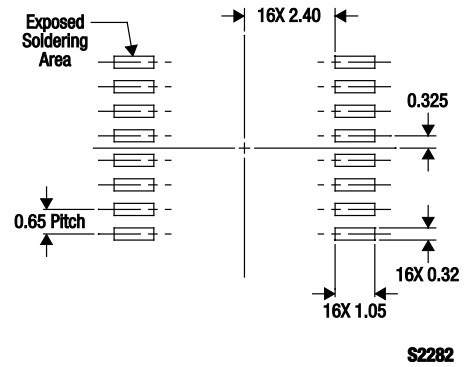


Figure 34. Think Shrink Small Outline Package (TSSOP) (16-Lead, Exposed Pad)

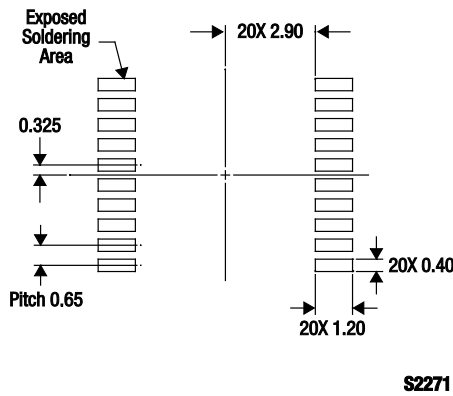


Figure 33. SSOP (20-Lead)

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