ANADIGICS’ AWB, AWM, and AWT series of Wireless Infrastructure/Small Cell Base Station and Mobile Power Amplifiers are high performance devices that deliver exceptional linearity and efficiency at high output power levels. The devices operate over the voltage supply range of +2.9Vdc to +4.5Vdc; and their output power handling capabilities increase as the supply voltage is raised towards the high end of their respective maximum operating range. At higher RF output powers, thermal considerations need to be taken into account in order to maintain the devices high level of reliability.

This application note addresses the thermal issues that need to be considered during the PCB design.

**PRINTED CIRCUIT BOARD THERMAL DESIGN CONSIDERATIONS**

The junction temperature ($T_J$) is defined as the maximum temperature present within the overall structure of the circuit that is fabricated onto the die. The “junction” refers to a point source that emanates thermal energy generated by the combination of DC and RF power dissipated by each active device that constitutes the primary circuit within the amplifier module.

The case temperature ($T_C$) is defined as the external temperature of the bottom surface of the package. This bottom surface is comprised of gold-plated copper and is the main facilitator of thermal energy transfer from the die to the PCB mounting area and heatsink. All thermal calculations are referenced to the case temperature ($T_C$) because it can be directly measured with the appropriate instrument. Conversely, the junction temperature ($T_J$) can only be calculated indirectly as the die is normally inaccessible.

In general, it is essential to keep the junction temperature ($T_J$) of the device as low as possible in order to ensure long operating life. This can be accomplished by providing good thermal relief and adequate heat sinking. When mounted to a printed circuit board (PCB), the delta between the device case temperature ($T_C$) and the ambient temperature will be determined by several factors; board thickness and number of layers, copper plating thickness, size and number of vias placed beneath the ground area of the case, the PCB layout, the method of attachment of the PCB to the heat sink as well as the design of the heat sink. For typical applications, it is recommended to maximize the number of vias placed below the package ground area.

Our standard AWB, AWM, and AWT evaluation boards are fabricated using Rogers R4003 PCB material which has a dielectric constant of 3.55, dielectric thickness of 8mils (0.2mm), and copper thickness of 1.4mils/side (0.0356mm). As the package size varies depending on the device type, the chart below can be used to determine the approximate number of vias that should be placed beneath the bottom ground area of the IC. Please consult the Appendices at the end of this document for the recommended Solder Stencil Aperture, PCB Footprint, and Solder Mask dimensions for both the 4x4mm and the 7x7mm packages.

<table>
<thead>
<tr>
<th>Package Type</th>
<th>4x4mm</th>
<th>7x7mm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total # of Vias</td>
<td>28</td>
<td>59</td>
</tr>
</tbody>
</table>
Thermal Design for the AWB, AWM and AWT series of Power Amplifier Modules

Figure 1: PCB Via Hole Layout for 4x4mm² Package (28 Vias)

Figure 2: PCB Via Hole Layout for 7x7mm² Package (59 Vias)
The physics of heat transfer

Conductive heat transfer or flow (Q) across any interface is given by the equation:

\[ Q = kA \Delta T / L \]

where:
- \( Q \) = heat flow
- \( k \) = thermal conductivity (of the material), W/mm °C
- \( A \) = area (cross section) of the heat flow path, mm²
- \( L \) = interface thickness (path length), mm
- \( \Delta T \) = temperature difference (drop) across the interface, °C

The thermal resistance \( R_t \) is analogous to electrical resistance and is defined as:

\[ R_t = \Delta T / Q \]

Substituting, we have:

\[ R_t = L / kA \] (°C/W)

For a surface mounted part, the total thermal resistance \( R_t \text{-tot} \) consists of the path from the Amplifier Die through the die-attach \( R_t \text{-dat} \) and the bottom surface of the package \( R_t \text{-pkg} \), through the PCB solder \( R_t \text{-sld} \), then through the PCB vias \( R_t \text{-pcb} \), and finally through the bottom interface \( R_t \text{-int} \) to the Heatsink. This path (from the die to the bottom surface) is the primary conduit for conduction of thermal energy. Very little thermal energy is conducted out to the top of the package or to the sides of the package because the moulding compound filler material that occupies the otherwise empty internal volume of the package possesses poor thermal conductive properties.

Thus the total heat path thermal resistance is:

\[ R_t \text{-tot} = R_t \text{-dat} + R_t \text{-pkg} + R_t \text{-sld} + R_t \text{-pcb} + R_t \text{-int} \]

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**Figure 3: Thermal Resistances**
Thermal Design for the AWB, AWM and AWT series of Power Amplifier Modules

THERMAL RESISTANCE OF THE PCB

The thermal resistance of a single copper via (not solder filled) can be calculated as:

\[ \theta_{\text{via}} = \frac{L}{\sigma \pi (R_o - R_{\text{pl}})^2} \]

For a via path length \( L = 0.274 \text{mm} \), with drilled hole radius \( R_o = 0.15 \text{mm} \), copper plating \( R_{\text{pl}} = 0.036 \text{mm} \), and copper thermal conductivity \( \sigma = 0.39 \text{W/mm}\degree\text{C} \), the thermal resistance of each via is 22.39°C/W. Therefore, the \( \theta_{\text{PCB}} \) using 28 non-solder filled vias is approximately 0.8°C/W.

For solder-filled vias, the thermal resistance of the solder fill can be calculated as:

\[ \theta_{\text{solder fill}} = \frac{L}{\sigma_{\text{solder}} \pi (R_o - R_{\text{pl}})^2} \]

The thermal conductivity of solder \( \sigma_{\text{solder}} = 0.05 \text{W/mm}\degree\text{C} \), the thermal resistance of each solder fill is 134.22°C/W. Therefore, the total \( \theta_{\text{solder fill}} \) for all vias on the pcb will be: 134.22 / 28 = 4.79°C/W.

Combining the thermal resistance of the vias and the solder fill, the overall \( \theta_{\text{PCB}} \) with 28 filled vias will be 0.69°C/W.

THERMAL RESISTANCE OF THE SOLDER INTERFACE

Solder is the most commonly used interface between the bottom grounding surface of the package and the via-holes that comprise the thermal-transfer area of the PCB footprint. The thermal resistances of the solder attachments \( (R_{l-\text{slid}}) \) are calculated below for both 4x4mm and 7x7mm packages with bottom grounding-surface areas of approximately 9mm² and 37mm², respectively. A solder thickness of .025mm is assumed for both packages. This magnitude of thickness is considered be to be a well executed solder attachment.

<table>
<thead>
<tr>
<th>Package Type</th>
<th>4x4mm</th>
<th>7x7mm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ground Surface Area (mm²)</td>
<td>9</td>
<td>37</td>
</tr>
</tbody>
</table>

\[ R_{l-\text{slid-4x4}} = \frac{L}{kA} = \frac{0.025}{(0.050 \times 9)} = 0.056 \degree\text{C/W} \]

\[ R_{l-\text{slid-7x7}} = \frac{L}{kA} = \frac{0.025}{(0.050 \times 37)} = 0.014 \degree\text{C/W} \]

As can be seen from the above numbers, the added thermal resistance from the solder attach is about two orders of magnitude smaller than that of the vias, and can be safely ignored (as long as the solder is kept to minimum thickness).

THERMAL RESISTANCE OF THE HEATSINK COMPOUND AND GASKETS

The PCB-to-heatsink interface \( R_{l-\text{int}} \) can be similarly calculated, but will vary according to the attachment method used (heatsink compound or gasket) and is hard to quantify (because the average L depends on the smoothness of the heatsink surface). It should be remembered, that the best of heatsink compounds exhibit a k value in the 0.001 to 0.007 W/mm °C range and that the typical 0.2mm thermal gasket sheet such as the Laird TFlex™ series has a k value of approximately 2 W/mm °C (vs. 0.390 W/mm °C for copper). Therefore, tight fit (screw down) and a smooth surface are important, but in any case, the \( R_{l-\text{int}} \) is still a small fraction of the total \( R_l \).

Any decrease in the PCB \( R_l \) due to heat transfer in the PCB material can also be ignored due to its poor heat conductance.

HEAT RISE

Finally, knowing all of the thermal resistances we can calculate the resultant temperature difference between the grounding surface on the bottom of the package and the heatsink. For example, using ANADIGICS AWB7227 power amplifier module that draws about 750mA @ 4.5Vdc with a total power dissipation of approximately 2.9W, a PCB with 59 non-solder filled vias configured as shown in Figure 2, will be about 0.38°C/W * 2.9W = 1.1 °C rise for the solder and PCB mount interfaces, the total temperature rise will be less than 3 °C.

The maximum operating case temperature (Tc) for the AWB7227 device is specified as +85 °C, so it can be seen that should the heatsink (ambient) temperature ever rise to +70 °C a safety margin of more than some 10 °C would still exist.
Appendix 1: 4x4 Package

NOTES:

1) UNLESS SPECIFIED DIMENSIONS ARE SYMMETRICAL ABOUT CENTER LINES SHOWN.

2) DIMENSIONS IN MILLIMETERS.
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2. DIMENSIONS IN MILLIMETERS.

3. VIAS SHOWN IN PCB METAL VIEW ARE FOR REFERENCE ONLY. NUMBER & SIZE OF THERMAL VIAS REQUIRED DEPENDENT ON HEAT DISSIPATION REQUIREMENT AND THE PCB PROCESS CAPABILITY.

Appendix 2: 7x7 Package
Appendix 3: 7x7 Package (with Ground Pad Notches)

NOTES:

(1) UNLESS SPECIFIED DIMENSIONS ARE SYMMETRICAL ABOUT CENTER LINES SHOWN.

(2) DIMENSIONS IN MILLIMETERS.

(3) VIAS SHOWN IN PCB METAL VIEW ARE FOR REFERENCE ONLY. NUMBER & SIZE OF THERMAL VIAS REQUIRED DEPENDENT ON HEAT DISSIPATION REQUIREMENT AND THE PCB PROCESS CAPABILITY.
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